Moving Towards High Carrier Mobility Power Devices in Silicon and Silicon Carbide

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"We choose to go to the moon. We choose to go to the moon in this decade and do the other things, not because they are easy, but because they are hard, because that goal will serve to organize and measure the best of our energies and skills, because that challenge is one that we are willing to accept, one we are unwilling to postpone, and one which we intend to win, and the others, too."

John F. Kennedy

Abstract

This thesis reports on recent progress regarding the characterization, design and fabrication of modern power semiconductor devices in Silicon (Si) as well as in the promising wide band gap material Silicon Carbide (SiC). Up to now, state of the art power devices are architectured on the basis of monocrystalline Si-wafers. This is due to the high material quality of Si in combination with the availability of a mature and reliable fabrication technology based on a well-established process library. However, more and more sophisticated device designs such as *e.g.* the Super-Junction (SJ) architecture require an increasing number of fabrication steps therefore increasing the amount of possible sources of error. Further, more complex three-dimensional dopant distribution profiles are needed for the devices to withstand the high blocking voltage demands of current power semiconductor applications when operated in reverse direction. This dopant distribution has to be monitored, at least for control samples, after implantation, after further thermal processes and during the duty cycle. To ensure reliable device operation, in particular for charge compensated devices, this monitoring or mapping has to be performed locally with high precision and sensitivity.

In this work complementary Scanning Probe Microscopy (SPM) based methods like: Kelvin Probe Force Microscopy (KPFM), Scanning Capacitance Force Microscopy (SCFM) and Scanning Spreading Resistance Microscopy (SSRM) have been explored for a precise monitoring of carrier concentration profiles. This is due to the fact that so far none of the established industrial techniques such as *e.g.* Secondary Ion Mass Spectrometry (SIMS) or Spreading Resistance Probe (SRP) was mature enough to simultaneously full-fill all the major requirements of the semiconductor industry in terms of spatial resolution, sensitivity, reproducibility and the ability to quantify dopant concentrations. Further, SIMS is probing the chemical composition rather than the charge carrier distribution. To 'look inside' the inhomogeneously doped sample, smooth device cross-sections need

to be prepared in a reliable manner and without distorting the 'as implanted/activated' dopant profile. In this way artefacts arising from a topographic signal can be ruled out. For Si the easiest way would be to cleave the wafer along a certain crystallographic direction. However, since the SPM methods presented here shall serve as a characterization tool with a general validity another approach that is also suitable for different crystal structures and materials with a hardness close to diamond had to be found. For this reason a chemical mechanical polishing (CMP) procedure had been developed at PSI. This process was optimized for maintaining a low surface state density as it is important to avoid a complete pinning of the Fermi level for the KPFM measurements. The subsequent Atomic Force Microscopy (AFM) imaging has been performed in collaboration with the experts in the research group of Prof. Ernst Meyer at the University of Basel.

Within this project it has been demonstrated that every SPM derived method is capable to qualitatively map carrier concentrations down to an unprecedented low regime. However, a difference regarding the lateral resolution was observed which can be understood by different information depths depending on the underlying physical quantity to be measured together with an imperfect surface preparation which is leading to an accumulation or depletion of defects at the surface. The most critical technique in that sense - due to its high surface sensitivity - is the contact potential difference measurement that is utilized by KPFM to draw conclusions on the carrier concentration. By laser illumination of the sample during the KPFM experiment a Surface Photo Voltage (SPV) occurs in a surface near layer with a thickness in the order of the minority carrier diffusion length. Thus, the surface sensitivity is reduced and the signal distortion due to the unfavourable influence of surface defects gets less pronounced. Even though SCFM is also based on the detection of the electrostatic force that develops between the tip and the sample, this method is less affected by the surface because it is probing a different physical quantity, namely the total capacitance of the rather extended oxide/depletion layer capacitance system. Furthermore, the magnitude of the SCFM signal scales inverse proportionally with respect to the carrier concentration, hence this method is theoretically offering the highest sensitivity in the low concentration regime. Nevertheless, a quantification scheme for this technique is still in development and further work on locally acquired spectroscopic capacitance-voltage (C-V) measurements is needed towards a reliable quantification procedure. The third SPM derived method SSRM, is operated in contact mode under high normal forces to ensure that the spreading resistance is the dominant resistance contribution for the current flowing between the tip and the sample. Under these circumstances the local carrier concentration and its impact on the magnitude and the sign of the output current can be investigated in a very accurate and quantitative manner. Beside that, the high mechanical forces cause an abrasive motion of the tip while scanning the sample. This feature is beneficial in two ways: on one hand the native oxide and the underlying defect-rich surface layer are removed while on the

other hand a phase transformation of a tiny sample volume just below the tip occurs which locally decreases the resistivity and increases the spatial resolution. Hence, the SSRM technique is showing a high degree of reproducibility and is therefore ideal for quantitative studies.

As mentioned above the considerable complexity of the fabrication process and the limited material properties of Si in terms of a high critical electric field and a high thermal conductivity accelerated the search for novel substrates for power semiconductor applications. Beside offering an order of magnitude higher critical electric field due to its wide band gap (WBG), SiC also attracted attention since it can be thermally oxidized resulting in a silicon dioxide (SiO_2) layer as its native oxide. Therefore, this material has been classified as most promising and theoretical improvements of a - by a factor of 400 - lower ON-resistance have been calculated. However, to date SiC devices are facing other problems related to the engineering of dopant profiles and the more complex nature of the oxidation process which limit their performance and hinder their large-scale commercialization.

The incorporation of a specific dopant distribution in SiC is most effectively done by an ion implantation process followed by a high temperature annealing step which is needed to restore the crystal structure after implantation-induced damage and to electronically activate the dopant atoms. This is caused by the fact that in SiC due to its wide band gap of 2.4-3.2 eV (depending on its poly-type) basically no dopant diffusion at reasonable thermal budgets occurs. Notably, not all of these dopant atoms are ionized and contribute to the electric conduction within the semiconductor. Especially the hole concentration p and the acceptor concentration N_A can differ significantly in SiC due to the large ionization energies. Hence it has to be taken into account that the final performance of a SiC power device might be inferior to the expected performance from the implantation parameters. This behaviour is in clear contrast to Si where at room temperature basically all donor and acceptor atoms are ionized and no further differentiation between the dopant and the carrier (electronically active dopant) profile has to be made. The above mentioned SPM methods are sensitive to the carrier rather than to the dopant profile and within this work it has been demonstrated that *e.g.* the p-doped guard ring structure of a SiC Schottky diode which is shielding the metal contact from high electric fields that occur under reverse bias operation can be resolved.

Another challenge for SiC Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices are low carrier mobilities inside the thin conducting channel at the semiconductor/oxide interface and threshold voltage instabilities. Due to the more complex nature of the oxidation process which requires the removal of carbon atoms in the form of CO or CO_2 from the SiC crystal the SiC/SiO_2 interface is showing a high density of interface trap states that act as scattering centres and degrade the carrier mobility. Hence, experimentally observed charge carrier mobilities are by a factor of 10 below

the theoretical value of the bulk material. Thereby the ON-resistance which is inverse proportional to the mobility is increased which is leading to a higher amount of power dissipation in the ON-state of the device. Unsurprisingly, a lot of research effort has been triggered in this direction resulting in breakthrough called post-oxidation annealing (POA) under gaseous ambients. Nitrogen and phosphorous based chemistries have shown a passivating effect on the density of interface trap states. However, the origin of this mechanism is not yet fully understood. A possible explanation is a counter-doping effect within a thin layer at the semiconductor surface.

A second - maybe easier - pathway to increase the channel mobility is the utilization of the crystal anisotropy. The mobility strongly depends on the orientation of the channel with respect to the crystallographic axis. Among them the $\{11\bar{2}0\}$ direction exhibits the highest mobility. In the here presented project this approach has been utilized to improve the device performance without changing too many parameters regarding the oxidation or post-oxidation treatments at the same time. In this case the remaining challenge was to develop an etching process which is able to etch several μm deep trenches into SiC and to precisely control the shape of the resulting trench profile. It has been demonstrated that sharp corners that would cause field crowding at the edges can be eliminated by the usage of very small DC biases applied between the electrode of the plasma chamber and the substrate. Furthermore, the steepness of the sidewalls could be controlled by the composition of the plasma gas flows. Contrary to previous reports we found that the addition of oxygen to the dry etching process is not helping to avoid microtrenching. Either a pure SF_6 based process or an SF_6 based process with the addition of Ar have shown the best results. With this success a full manufacturing cycle for a nanoscale trench MOSFET has been designed.

This dissertation is dedicated to my mother for her ongoing love and support and to the memory of my beloved father who could not see this thesis completed.

Preface

The research area of solid state physics is offering an interesting playground for experimental physicists since many different disciplines within this superordinate field that are in a constant interplay with each other have to be taken into account for a precise description of nature in terms of *"the study of matter, energy and the interaction between them"* as it is stated in one of the definitions of physics.
Within the scope of this thesis the concepts of surface science and semiconductor physics and manufacturing have been brought together to overcome certain challenges of state of the art power semiconductor devices. Didactically the frame of this work embraces fundamental solid state physics, semiconductor device engineering and the - from a textbook perspective - existing gap between them to be directed towards a broader audience even without the requirement of a too specific background knowledge in either of these fields.
The content itself will be organized in a chronological order according to the different research projects that have been conducted during my PhD time at the Paul Scherrer Institute. In other words, after giving an introduction to the existing challenges and to the methods used for characterization, the thesis will be split into two parts. The first one adresses the imaging and the analysis of electronically active dopant profiles also including sample preparation routines while the second one covers the design and the different processing steps towards novel prototype trench MOSFET devices in SiC. As part of the "Nano-Argovia" programme of the Swiss Nanoscience Institute (SNI) both topics have been investigated in close collaboration together with the University of Basel as academic and ABB as industrial partner. For the second project experts from the CSEM Muttenz complemented our research consortium.

Contents

List of Abbreviations

The following table contains an alphabetically ordered list of abbreviations used throughout this thesis:

Methods

AFM	Atomic Force Microscopy
CMP	Chemical Mechanical Polishing
C-V	Capacitance-Voltage
ICP	Inductively Coupled Plasma
I-V	Current-Voltage
KPFM	Kelvin Probe Force Microscopy
MP	Mechanical Polishing
nc	non-contact
POA	Post Oxidation Annealing
RIE	Reactive Ion Etching
SCFM	Scanning Capacitance Force Microscopy
SEM	Scanning Electron Microscope
SEPC	Secondary Electron Potential Contrast
SIMS	Secondary Ion Mass Spectrometry
SPM	Scanning Probe Microscopy
SPV	Surface Photo Voltage
SRP	Spreading Resistance Probe
SSRM	Scanning Spreading Resistance Microscopy
TCAD	Technology Computer Aided Design

Devices

AC	Alternating Current
BG	Buried Grid
BJT	Bipolar Junction Transistor
DC	Direct Current
GTO	Gate Turn Off Thyristor
IGBT	Insulated Gate Bipolar Transistor
JBS	Junction Barrier Schottky
MISFET	Metal Insulator Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SBD	Schottky Barrier Diode
SCR	Space Charge Region
SJ	Super Junction

Materials

Al	Aluminum
Al_2O_3	Aluminium oxide
Cr	Chromium
GaAs	Gallium arsenide
GaN	Gallium nitride
Ge	Germanium
InP	Indium phosphide
PMMA	Polymethylmethacrylat
Ni	Nickel
Si	Silicon
SiC	Silicon carbide
SiO_2	Silicon dioxide

CHAPTER 1

Introduction to modern power semiconductor devices

1.1 Historical overview

The rich and complex history of semiconductor physics among many other disciplines is far away from following a straight line in its development and progress [1–3]. It rather took many unexpected turns. In one case the term 'renaissance' is even used [1] which is due to the fact that early stage semiconductor detectors couldn't compete with vacuum electron tubes in terms of reliability. Later on however, semiconductors outperformed thermionic valves in many application sectors because technological obstacles were overcome which enabled a more reliable operation. Another nice example of the sometimes difficult to predict turns of technological evolution is given by a quote that dates back to the year 1943 and is attributed to Thomas J. Watson Sr., who was the founder and then CEO of IBM:

"I think there is a world market for about five computers."

Notably, there is no other company that later on contributed so much to the successful integration of personal computers into people's homes than IBM. Unsurprisingly numerous challenges from the physical understanding towards device applications still needed to be overcome until the former statement by Mr. Watson was eventually falsified and the new era of the so called "Silicon age" began.
Before discussing which material fits which application best, the discovery of fundamental semiconducting properties needed to be well understood. Even though the development of first semiconductor devices took place - from a chronological point of view - often in parallel, in the following paragraphs they are described separately.

1.1.1 Physical concepts

The three most fundamental properties attributed to semiconductors are:

1. an increasing conductivity with temperature
2. a light induced photo-conductivity

and

3. a conductivity which depends on the presence of impurities/dopants

ad 1)
The term materials of semiconducting nature, dates back to the work of A. Volta in 1782 [4], who observed that the discharge speed of an electro-meter depends on the nature of the material brought in contact with it. The discovery however, of one of the characteristic properties of semiconductors, namely the increase of the conductivity at higher temperatures, is attributed to M. Faraday [5] in 1833. He recognized that the conducting power of silver sulfide (Ag_2S) or the 'sulphuret of silver' as he called it was increased when the temperature is increased. This behaviour was contrary to that primarily observed for metals [6].
In the original publication [5] he described this effect as follows:

"When a piece of this sulphuret, half an inch in thickness, was put between surfaces of platina, terminating the poles of a voltaic battery of twenty pairs of four-inch plates, a galvanometer being also included in the circuit, the needle was slightly deflected, indicating a feeble conducting power. On pressing the platina poles and the sulphuret together with the fingers, the conducting power increased and the whole became warm."

Further, he found that this effect was enhanced by putting a lamp in close proximity to the Ag_2S and the conductivity of this material became similar to those of metals. This effect was reversible and under ideal conditions (good contact with the platina poles, freshly charged battery, initial temperature not too low) the Joule heating of the current was enough to provoke this behaviour.
However, the underlying mechanism kept researchers puzzling for several decades. Only a better understanding of the transport properties of charged particles in terms of their resulting electrical and heat current [7] together with the discovery of the electron by J.J. Thomson [8] in 1897 opened up a pathway for the theoretical formalism by the Drude-model [9] of the free electron gas. In this model the electrons can move freely in analogy to gas molecules inside an ideal gas. The success of this model in describing the empirically found ratio between the thermal and the electrical conductivity that

is known as Wiedemann-Franz law [10] inspired Koenigsberger and his coworkers to a dissociation theory for electrons in semiconductors [11]. According to the value of the dissociation energy q which is needed to separate an electron from the corresponding atom the number of free electrons that are conducting a current varies as given by the formula:

$$N = N_0 e^{-\frac{q}{T}} \tag{1.1}$$

where: N = number of free electrons
N_0 = total number of electrons
q = dissociation energy
T = temperature

In the limiting case of very high temperatures or small values of q, $N = N_0$ as it is the case for metals. Once these electrons are contributing to the conductivity their behaviour was expected to be the same as for electrons in metals. Therefore, for the first time a relation for the conductivity in variable conductors could be derived, since the conductivity was thought to be directly proportional to the number of the dissociated electrons.

ad 2)
Another property that is characteristic for semiconductors is the dependence of their electronic behaviour on the absorption of light. In Becquerels experiments with electrolytes in 1839 he was using a silver chloride (AgCl) coated platinum electrode resulting in a semiconductor/electrolyte junction. He recognized that upon illumination with sunlight the electromotive force of the cell was changed by the induced photovoltage. The observation of an analogeous effect in solids was made by W. Smith [12] in 1873. He was originally working on submarine cables for telecommunication applications and looking for a highly resistive and reliable resistor. In the conducted resistance measurements for Selenium bars he found that there was a large scatter of the experimental results that was independent of the operator. In his work [12] he described the situation as such:

"While investigating the cause of such great differences in the resistances of the bars, it was found that the resistance altered materially according to the intensity of light to which they were subjected. When the bars were fixed in a box with a sliding cover, so as to exclude all light, their resistance was at its highest, and remained very constant, fulfilling all the conditions necessary to my requirements; but immediately the cover of the box was removed,- the conductivity increased from 15 to 100 per cent, according to the intensity of the light falling on the bar."

Further, by putting his experimental setup into a trough of water he was decoupling this photoconductive effect by possible infulences from temperature related phenomena.

On the basis of this discovery, Adams and Day did a very systematic study on the influence of light on Se [13]. They investigated among other characteristics the influence of the light source and found that the change in resistance is directly proportional to the square root of the illuminating power. Their greatest achievement however was that they could answer the question if the action of mere light on Se is sufficient to generate an electrical effect. Their positive answer opened up further research and is considered as the beginning of photovoltaics.

ad 3)
Last but not least in the following paragraph the controlled tuning of the conductivity of semiconductors shall be discussed. The incorporation of impurities which is known as doping of semiconductors is one of the fundamental ways to control the conductivity and other electronic and optical characteristics of these materials. Therefore the device functionality crucially depends on the underlying dopant or carrier profile which renders the manufacturing and the characterization of such profiles. This topic of utmost importance provides the main content of this thesis.
Historically, the dopant effect in semiconductors has primarily been systematically investigated by K. Baedeker [14]. In his well-engineered experimental setup he was able to produce thin compounds by first sputtering a metal onto a glass substrate followed by an exposure to air or gaseous ambients such as *e.g.* the vapour of iodine. His most famous work was on copper iodine (CuI) that showed a modest conductivity in its 'pure' state but an increased conductivity when the stoichiometry was changed and the iodine content was increased. By the interaction with saturated or diluted iodine vapour or solution the iodine content could be changed and monitored by precisely measuring the change in weight.
It was B. Gudden who then came up with the idea that the semiconducting properties of materials are caused by impurities [15] that are incorporated in their host crystal lattice. Further he believed that pure chemical substances will never show this effect. With this statement he referred to what is known today as extrinsic semiconductors. Even though his hypothesis turned out to be wrong and the existence of intrinsic semiconductors could be verified with the progressing research on the purification of Germanium (Ge) and Silicon (Si), his thoughts influenced other scientists in this field, among them A. Wilson.

A fundamental breakthrough in our understanding of the above mentioned properties was made when quantum mechanics found its way into the solid state and especially into semiconductor physics. In the beginning the Drude model for electrons in metals was extended by taking the Fermionic nature and therefore Fermi Dirac statistics into account. M. Strutt adressed the wave nature of the electron and applied it to a periodic potential [16]. These works influenced F. Bloch who found that the wave function of an electron in a periodic potential differs from the one of a free electron only by a

modulation factor with the periodicity of the crystal lattice [17]. If this ansatz was then put into the Schrödinger equation and solved with respect to its eigenvalues he found that there is a difference to the free electron case at the Brillouin zone boundary where two different bands are now formed. A similar effect at these boundaries was found by the concept of Peierls [18] in the case of nearly free electrons that he analyzed by the means of perturbation theory. A. Wilson in the end was putting these pieces together and formulated the band theory for electronic conduction in semiconductors [19].

1.1.2 Evolution of semiconductor devices and substrates

The second part of this historical overview shall now focus on early stage semiconductor devices and on their evolution upon technological progress which was mainly due to advanced fabrication techniques which in the end were able to produce highly pure Ge and Si substrates.

As stated above, semiconductor device development - even though sometimes without understanding the physical mechanism of the working principle - took place basically in parallel to the conceptual understanding of the nature of semiconductors. The first semiconductor rectifier was actually built by C.F. Braun in 1874 [20] who was conducting research on the conductivity of metal sulfides of different purities which he contacted with thin metal wires. He recognized that the resistance was depending on the direction, the intensity and on the duration of an electric current flow. At that time the discovery of rectifying properties did not find much appeal. Only the discovery of electromagnetic waves opened up an application for the so called cat's whiskers detectors (the name arose due to the similarity of the thin metal wires).
Another example for a semiconducting device of the 19th century is the first cell that made use of the photovoltaic effect [21]. Based on the results of Se research [12, 13] upon light absorption, Fritts assembled a photovoltaic cell that was made of a thin layer of molten Se that was put between a metal substrate and a thin gold top electrode. Through the thin gold layer light absorption could take place and showed - even though with a very small efficiency - the desired effect.
The increasing interest in radios in the beginning of the 20th century triggered more and more research towards the direction of semiconductor rectifiers. In this context, emphasis shall be put on the work by Pickard who systematically investigated a large number of different materials in terms of their applicability for radiowave detection. Within this framework, the first patent for a Si point-contact rectifier was filed [22]. However, at this time semiconductor rectifiers were outperformed by thermionic valves. They were much less sensitive to external influences which was one big disadvantage of the point-contact nature of the semiconductor counterparts. The often defective device behaviour and at that time a not well understood theory might stinged Pauli to the

following statement:

"One shouldn't work on semiconductors, that is a filthy mess; who knows if they really exist?"

This erratic behaviour was also recognized by Ohl in 1935 [23] who tried to avoid these random fluctuations in their behaviour by melting raw Si in quartz tubes. The obtained ingot after the solidification was still polycrystalline but now showed a much more homogeneous behaviour in terms of its rectification properties. Accidentally, he also discovered a photovoltaic effect in Si which had been attributed to a junction formed inside. With the ongoing research he found that due to the segregation of impurities during the solidification a 'purified' and a 'commercial' end of the rod was created. Upon further research it was found that this was due to the different weight of impurities. Dependent on their easy direction of current flow with respect to the applied voltage the different types of Si were called p or n-type. Hence, the pn junction was born.
Following to these fundamental insights into impurity elements and semiconducting elements, also in the context of their position in the periodic table, also Germanium gained more and more attention since it had a lower melting point and it was less reactive than Si at elevated temperatures. Furthermore, Ge exhibited a higher mobility than Si which was favourable for the detection of microwaves since it led to higher cut-off frequencies. The disadvantage of a smaller bandgap in terms of thermal stress was acceptable. These advantages and the increasing knowledge regarding a high quality crystal growth then later on led to the invention of the first point-contact transistor in 1947 by Schockely, Bardeen and Brattain [24]. Its working principle was based on the field effect meaning that an electric field was used to control the shape and the conductivity of the channel.

The first working transistor was a proof of principle with the goal to show that also a semiconductor equivalent of the controllable thermionic valve is possible. However, the production of this point-contact devices was not very reproducible due to the nature of the polycrystalline substrate that was used. Scattering effects at the grain boundaries occured and as their consequence devices significantly differed in their performance. The need of a high-quality single crystalline material was recognized by G. Teal and his coworkers, who setup a growth process based on the Czochralski method [26]. They used a small piece of single crystalline Ge as a structural template for molten polycrystalline Ge. By a variation of the pulling speed larger diameters of the ingot could be realized. Further, by adding donor or acceptor elements, differently doped layers could be manufactured. The direct consequence of this technological progress was the fabrication of a junction transistor [27] and later on of an alloyed transistor [28] whose fabrication was more suitable towards a large-scale commercialization.
The interest in Si later on arose again due to its larger band gap which was more suitable for power applications due to a higher robustness in terms of thermally generated leak-

Figure 1.1: An enlarged replica of the first Germanium point-contact transistor (Figure taken from Ref. [25]) consisting of a triangle with gold contacts, that is pressed upon the n-type germanium. Below a copper contact serves as base terminal.

age currents in the OFF-state of the device. However, according to Ref. [29] this was not enough to replace the existing Ge technology. Rather two different discoveries were initiating the Si age that we are facing today. The first one is connected the passivating property [30] of SiO_2 on surface states that are due to dangling bonds of a terminated Si single crystal. This led to a high quality oxide/semiconductor interface enabling the control of charge carriers through the oxide in Metal-Oxide-Semiconductor (MOS) systems. The next logical step was to extend the existing concept of FETs with this newly found feature. With the first implementation of a Si Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) [31] the triumph of Si slowly began. The second important discovery for Si is provided by the integration capability in the form of integrated circuits which has primarily been investigated by Kilby [32], who recognized that the wire connection between individual devices was causing major problems. The usage of SiO_2 as mask material for different types of lithography was key towards further processing steps.

1.1.3 Compound semiconductors beyond Silicon

The last part of this section is focussed on building a bridge between developments beside Si technology and current power electronics research. Depending on the type of application the material properties of Si are limited in terms of *e.g.* high frequency or high temperature applications. Further, the yield of optoelectronic devices is enhanced in the case of a direct band alignment between the conduction band minimum and the valence band maximum [29]. Therefore, material scientists always kept looking for materials

with beneficial properties depending on the device application, despite the success of Si. In this context compound semiconductors such as III-V or IV-IV compounds gained more and more attention.
Power applications require a high critical electric field to withstand large breakdown voltages when the device is operated in reverse direction. Hence materials with a wide bandgap are more suitable than Si even though sophisticated device designs could partially compensate this drawback for Si devices. The energy-efficiency of those devices is suboptimal however, and the room for further improvements is quite limited. In the following table the most promising candidates to replace Si for power electronics are listed and compared in terms of their material properties [33]:

Property	Si	GaAs	GaN	3C-SiC	6H-SiC	4H-SiC
Bandgap, E_g [eV]	1.12	1.43	3.4	2.4	3.0	3.2
Critical electric field, E_c [MV/cm]	0.25	0.3	3	2	2.5	2.2
Thermal conductivity, λ [W/cmK]	1.5	0.5	1.3	3-4	3-4	3-4
Electron mobility, μ_n [cm^2/Vs]	1350	8500	1000	1000	500	950
Hole mobility, μ_p [cm^2/Vs]	480	400	30	40	80	120
Dielectric constant, ϵ_r	11.9	13.0	9.5	9.7	10	10

Table 1.1: Comparison of material properties of different semiconductor substrates for power applications. All given values are measured at RT.

Even though the carrier mobility of wide bandgap materials is reduced compared to Si or GaAs, this disadvantage gets more than compensated by the one order of magnitude higher critical electric field as it can be clearly seen from the following formula for the specific ON-resistance [34]:

$$R_{ON} = \frac{4V_B^2}{\epsilon \mu_n E_c^3} \tag{1.2}$$

where: R_{ON} = ON-resistance
V_B = breakdown voltage
E_c = critical electric field
μ_n = electron mobility
ϵ = dielectric constant of the semiconducting material

The cubic dependence on the critical electric field of the denominator therefore gives rise to significantly lower values for the ON-resistance.
Notably, these values correspond to rather small and high quality samples. In terms of commercial devices the upscaling towards full wafers is required to establish this new

technology. A high quality single-crystalline bulk growth of SiC was for a long time a major obstacle since on the one hand the strength of the Si-C bond was disadvantageous and on the other hand the crystal structure needed to be precisely controlled. The latter is important since SiC crystals can occur with different crystal structures that exhibit different material properties. The so called polytypism is the variation of the crystal structure depending on the stacking sequence in one direction [35]. For SiC more than 200 polytypes are known [36].

In contrast to other semiconducting materials, a growth process from a stoichiometric melt is not possible at technologically relevant temperatures and pressures. Hence single-crystalline bulk SiC was obtained from a sublimation growth technique which goes back to Lely in 1955 [37]. In a graphite crucible SiC powder was heated to approximately 2500 °C until it sublimes. The mass transport of the sublimed species is governed by a temperature difference between the outer and the inner part of the crucible where single crystalline platelets are recrystallized. Even though the overall yield and the control of the polytypism were not very high, the material quality of the platelets obtained by this technique was high enough to use them as a seed for other growth techniques. Tairov and Tsvetkov developed an advancement based on the seeded sublimation growth [38] which is up to now the most widespread technique.

The polytype control of the single crystalline substrate was one of the major issues in SiC technology since the formation energy for stacking faults is low and therefore polytype mixing can easily occur [39]. Empirical relations for the stabilization of a certain polytype have been investigated and it was found that the polarity of the seed crystal as well as the C/Si ratio during growth are key for controlling the polytype of the growing substrate. Whether the bulk growth nucleates on a Si or a C face has therby the highest impact. The former favours the growth of 6H-SiC while the latter results in a 4H-SiC crystal [40].

The impurity doping also favours a certain polytype of SiC. This effect mainly depends on the site where the dopant is incorporated in the crystal. Nitrogen atoms *e.g.* occupy C lattice sites and therefore the growth atmosphere becomes C-rich which facilitates a 4H-SiC growth [41]. The opposite is true for Al which is incorporated as electron acceptor. Therefore the growth of p^+ 4H-SiC substrates by sublimation is still challenging.

Further, defects due to non-stable growth conditions such as *e.g.* micropipes compromise the subsequent homoepitaxial growth of the active device area. However, the ongoing research and development effort led to commercially available 6H-SiC in the beginning of the 1990ies. Together with the step flow control technique [42], which makes use of a certain off-angle to ensure a perfect control over the homoepitaxially grown polytype, the basis for SiC power devices was provided.

In retrospect there are similarities between the establishment of a Si-based technology and the obstacles SiC is facing today even though the processing technology is entirely

different. One of the biggest problems that SiC technology still encounters are the low observed channel mobilities for MOS-controlled devices. In contrast to Si where the passivation of surface states due to the SiO_2 layer was a breakthrough, the complex nature of the oxidation process is still hampering these kind of developments in SiC. Although passivating effects have been achieved by post oxidation annealing treatments the performance of SiC MOSFETs remained limited [43]. Within the fabrication related project of this thesis this problem has been addressed by the anisotropy of the channel mobility with respect to the orientation of the channel to a certain crystallographic axis.

1.2 Power devices and their power electronic applications

After the historical introduction and an insight into SiC technology within the following paragraphs and lines the focus shall be given to the application of power electronic devices. For this purpose a classification either on the current and voltage rating of the application or on the power and frequency rating of the underlying devices can be made.

1.2.1 Semiconductor power devices as building blocks for power conversion systems

Depending on the type of power conversion, there are four different possible systems. AC power can be either converted to DC power or to an AC output power with a different frequency or voltage. The situation is similar for DC power. Either the voltage of the DC power can be changed or it can be inverted towards an AC output signal.
There are various different converter types which realize the desired type of operation [44] but a detailed description would go beyond the scope of this thesis. However, the working principles of their major device building blocks shall be addressed here.
An AC to DC conversion is performed by the rectification property of a two-terminal semiconductor diode. Depending on the application this can either be done by a p-i-n diode or by a Schottky diode. The bias polarity of the source determines for both devices if they either are in their blocking (OFF-state) or in their conducting state (ON-state). Three-terminal devices have an additional control terminal which allows for a fully or semi-controllable operation. In Fig. 1.2 these power switches are categorized in terms of their power rating and in terms of their operating frequencies.

A brief description of the working principle of each of these devices will be given below [46, 47]:

P-i-n diode. The vertical structure of a p-i-n diode (see Fig. 1.3) consists of a narrow and highly doped p^+ region followed by the so called intrinsic region which is a lightly n-doped layer. At the end of this three layer structure is again an n-type layer but this time with a higher doping concentration. In principle this last layer would not be necessary for the desired rectification properties of the device. The contact formation to a lightly doped n-type layer however is suffering from high contact resistances. Therefore an additional highly doped layer gets introduced at the cathode side of the device. Depending on the dopant concentration of the intrinsic region there are two different designs of p-i-n diodes, namely the punch-through and the non-punch-through design. This term is referring to the breakdown electric field in reverse direction which is decreasing according to the dopant concentration of the intrinsic layer. If the concentration is low the field can penetrate into the n^+ layer. Due to the high concentration of this layer it

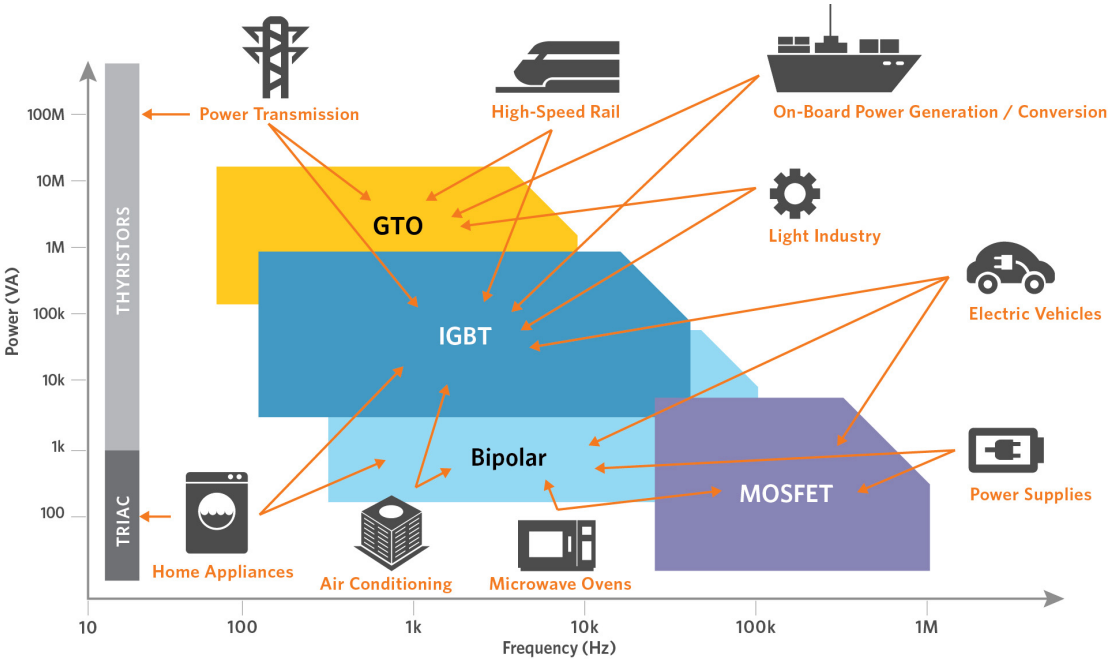

Figure 1.2: Classification of semiconductor power switches according to their power rating and operating frequency. Typical applications are indicated next to the device operating area inside the diagram. Figure taken from [45]

gets stopped on a short length scale inside this region. For higher dopant concentrations in the intrinsic layer the electric field does not penetrate into the n^+ region.

Schottky diode. In contrast to p-i-n diodes, the Schottky diode consists only of one impurity type inside the semiconductor. Most Schottky diodes are based on the junction of a metal with an n-type semiconductor (see Fig. 1.3) since the electron mobility is higher as compared to the one of holes. The rectification property of a Schottky diode is due to the Schottky barrier height of the metal semiconductor junction. While under forward bias the depletion zone inside the semiconductor is swept with electrons which reduces the effective barrier height the opposite takes place under reverse bias conditions and the depletion zone gets more extended. Due to the unipolar nature of this device the switching speed is higher as compared to p-i-n diodes. Design considerations in terms of a low forward voltage drop and in terms of a high breakdown voltage however resulted in a limit of 240 V for Si devices. Therefore soon the attention was given to wide band gap materials.

Bipolar junction transistor. The bipolar junction transistor consists of three differently doped regions that form either an *npn* (see Fig. 1.4) or a *pnp* structure. The different regions are named emitter, base and collector and can be regarded as two consecutive *pn* junctions. The working principle of an *npn* device can be understood as follows: if a negative voltage is applied to the emitter with respect to the collector no current is flowing since the base collector junction is reverse biased. If then a positive

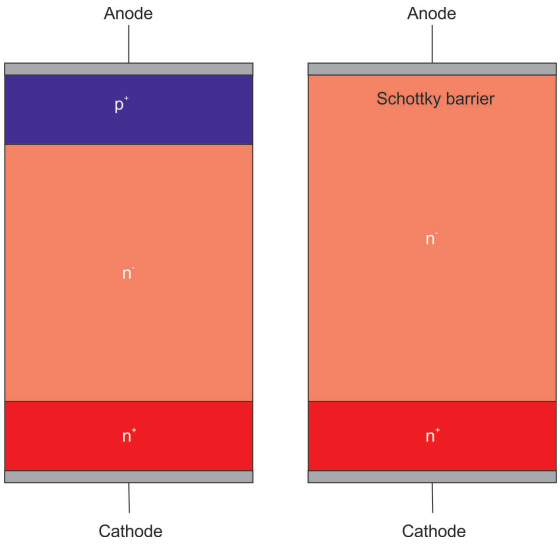

Figure 1.3: A schematic illustration of the cross-sections of a p-i-n (left) and a Schottky diode (right) is shown. While the rectifying nature of the p-i-n diode is caused by reverse biasing a *pn* junction, in the Schottky diode the barrier that forms at the metal semiconductor junction depends on the bias polarity.

voltage is applied to the base region with respect to the emitter the base emitter junction is forward biased and electrons get injected into the base and holes will flow towards the emitter. Due to recombination processes a lot of these injected carriers will be lost for the current transport. In the case of a narrow base region however a sufficiently large fraction can diffuse towards the base collector junction and will then be attracted by the electric field towards the collector. Hence by controlling the voltage across the base emitter junction the current flow through the initially reverse biased base collector junction can be controlled. If the voltage between the base and the emitter is later on again switched off the current flow between the emitter and the collector stops since no new carriers will be injected and the initial state is restored.

Thyristor. The thyristor can be regarded as a four layer *npnp* structure with a cathode (n) a gate (p) and an anode (p) terminal as shown in Fig. 1.5. If a positive voltage is applied at the anode with respect to the cathode the outer junctions are both forward biased while the whole reverse voltage is supported by the junction in the middle of this structure. To gain a better understanding on the operating principle the thyristor can be regarded as two bipolar junction transistors, where one of them is a *pnp* and the other one is an *npn* type. The application of a positive gate voltage to the p region of the second (*npn*) transistor with respect to the cathode is leading to a strongly forward biased collector-gate junction. Hence, electrons can diffuse through the gate towards second n-doped area which is at the same time triggering the n region of the first *pnp* transistor. Now holes can be injected that reach the collector of the first transistor. This current then adds up to the initial gate current. Due to this positive feedback

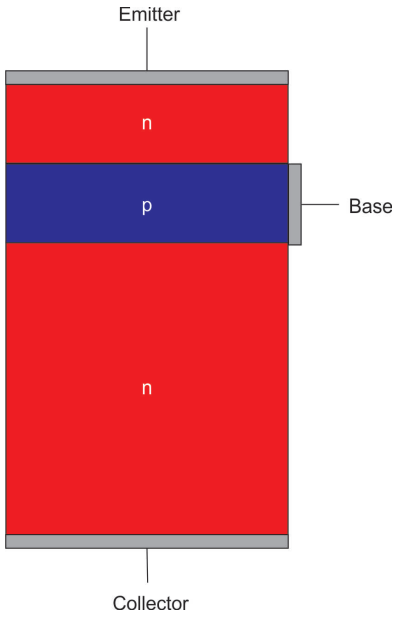

Figure 1.4: A schematic illustration of the cross-sections of a bipolar junction transistor is shown. Similar to the *npn* type depicted here also a *pnp* device can be realized by inverting the nature of the impurity atoms.

the thyristor remains in its ON-state even though the gate current is switched off. The device can be only switched off if the overall direction of current flow gets reversed. A special case of the thyristor is the Gate Turn off (GTO) thyristor which can be fully switched by applying a negative current to the gate.

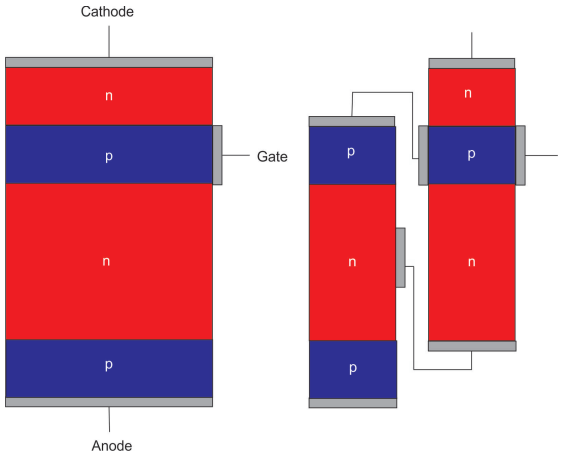

Figure 1.5: A schematic illustration of the cross-sections of the four layer *npnp* structure of a thyristor is shown. For a better understanding of the working principle the thyristor can be regarded as a composition of an *npn* and an *pnp* transistor.

MOSFET. As the name already suggests the operating principle of the power MOSFET critically depends on what is happening at the MOS interface. Depending on the carrier type which is conducting the current the MOSFET is categorized either as *n* or *p*-

channel. In the following, considerations regarding an n-channel MOSFET will be made which in a similar manner apply to the p-channel counterpart. In principle, a MOSFET is a four terminal device which consists of a source, a drain, a gate and a body terminal. In the n-channel case the substrate (body terminal) is p-doped with two n-wells at the surface that form the drain and source terminals (see Fig. 1.6). In order that a channel can form between drain and source, a gate terminal is needed to control the properties of the channel. This terminal is situated above the gate insulator which is SiO_2 in the case of Si or as well for SiC in the case of thermally grown oxides.
To understand the operating principle of a lateral MOSFET one has to consider two distinct electric fields, namely a transverse electric field which is caused by the potential difference between the gate and the substrate and a lateral electric field which is due to an applied voltage between the source and the drain region of the device. If a positive voltage is applied to the gate terminal with respect to the body majority holes will be depleted from the interface and minority electrons will be accumulated. Depending on the magnitude of this voltage an inversion layer of electrons can form below the gate oxide. This voltage is known as threshold voltage and enables a current flow between the source and the drain terminals if an appropriate drain-source voltage is applied. For the following considerations of the operating regimes the source and body terminals are grounded.
If the gate source voltage does not exceed the threshold voltage no inversion channel is formed and depending on the sign of the drain-source voltage the drain-body diode is either forward biased for negative V_{DS} resulting in $I-V$ characteristics of a pn junction or in the forward blocking state for positive V_{DS} where only a small leakage current will flow. In the latter case the depletion region widens into the channel.
If the gate source voltage is above the threshold voltage an inversion layer is formed below the oxide and electrons can flow from the source to the drain terminal. Depending on the magnitude of V_{DS} there are different operating regimes. In the linear regime a continuous channel gets formed. If the drain source voltage is further increased the increasing space charge region (SCR) of the reverse biased pn junction at the drain side leads to a constriction of the channel until the channel is not continuous anymore in the saturation regime.
For power applications however, mainly a vertical architecture with the drain contact on the backside of the wafer is used. With this geometry the cell pitch can be reduced as compared to the lateral counterpart which decreases the ON-resistance of the device. A special type of a vertical MOSFET is the Super-Junction (SJ) MOSFET [48] which is based on the charge compensation of alternating p and n-doped pillars inside the drift region (see Fig. 1.6). Due to the local charge compensation principle the drift layer exhibits a low effective dopant concentration which supports high voltages in reverse direction. In forward direction this design benefits by the fact that the single pillars

can exhibit a larger doping concentration as compared to drift layers in pn diodes and therefore the ON-resistance gets significantly reduced. While in conventional power MOSFETs the drift layer resistance increases by the desired breakdown voltage according to $U_{BR}^{2.5}$, this dependence gets diminished towards an almost linear behaviour for the SJ-MOSFET [49].

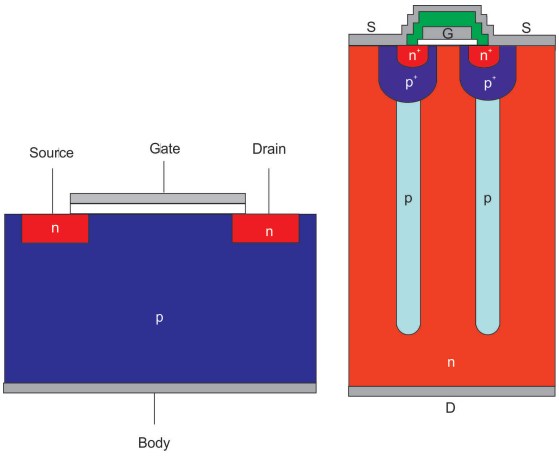

Figure 1.6: A schematic illustration of the cross-sections of a lateral MOSFET and of a trench MOSFET consisting of alternating n and p pillars is shown.

IGBT. The structure of an Insulated-Gate-Bipolar-Transistor (IGBT) is very similar to the one of a vertical double diffused power MOSFET. While in the case of the MOSFET electrons are injected through the p-well inside the drift layer and later on collected by a highly n-doped drain terminal, the IGBT employs a highly doped p-region at the back of the wafer as shown in Fig. 1.7. The establishment of a channel occurs analogously to the case of a MOSFET, only then when a gate voltage that exceeds the threshold voltage is applied. Electrons can now flow through the channel into the n-base region if a positive voltage is applied to the collector with respect to the emitter. At the same time holes get injected from the p-layer at the collector side which partially recombine with the injected electrons. The fraction of holes that does not recombine can reach the p-well of the pnp transistor structure.

1.2.2 Applications

As depicted in Fig. 1.2 there is a wide range for power semiconductor applications [41, 44, 50]. For lower power ratings such as for power supplies, power MOSFETs are used as converters since their fast switching speeds are reducing complexity of additional filtering components. Automotive electronics that are fed from the onboard power supply also make use of MOSFET based power switches.
For medium voltage drives that are connected to the grid an effective power conversion

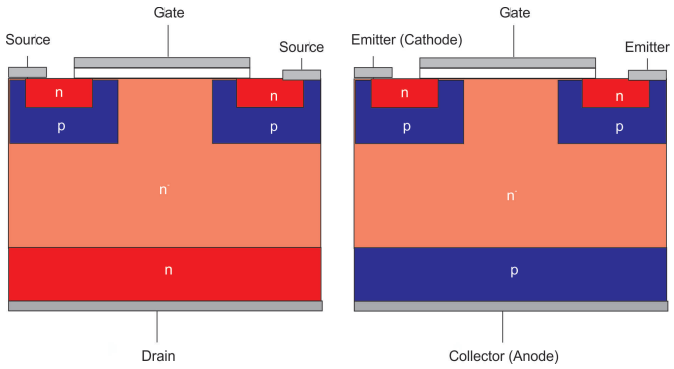

Figure 1.7: A schematic illustration of the cross-sections of a vertical MOSFET and of an IGBT is shown. The main difference is the dopant type of the layer near the backside contact.

is needed due to the different standards for power grids. The same applies for traction applications. Most common devices used for these application types are IGBTs since multi-axle designs (where more components are driven by the same converter) are more and more replaced by single-axle designs. Also the emerging photovoltaic applications need conversion from DC to AC to be fed into the grid which is most effectively done by IGBTs.

The high power spectrum is covered by thyristor based switches. If there is no constant operating speed of an engine or a turbine as it is the case for wind turbines, the generated power needs to be converted before it is fed into the grid. Another application in the high power regime is the high voltage DC transmission. Above distances from 800 km the higher costs of the DC terminal are redeemed by the lower line costs.

CHAPTER 2

Experimental techniques and processes

Within this chapter the experimental tools regarding the fabrication, preparation and characterization will be discussed in detail since the chapters 3, 4 and 5 which are based on published articles or final stage manuscripts are only refreshing this knowledge either by short paragraphs or by citing the appropriate references. The organization will thereby follow the structure of this thesis and not the life cycle of a device from its fabrication to its characterization.

2.1 Cross-section preparation

The requirement of a high blocking voltage capability when the device is operated under reverse bias conditions asks for rather complicated dopant architectures in modern power semiconductor devices. A plethora of devices therefore employs a vertical geometry that contains a thick drift layer to sustain high reverse voltages in addition to the device specific dopant distribution. Hence, in a first step, a cross-section of the device under investigation needs to prepared to reveal the dopant architecture below the wafer surface.

2.1.1 Chemical-mechanical polishing

The easiest method for the cross-section preparation would be the cleavage of the wafer along one of its crystallographic directions. This can be experimentally realized by scratching the wafer with a diamond scribe. In a second step two tweezers are used grab the corresponding halves of the wafer next to the groove. By the application of

a small mechanical force on the substrate the initial crack now propagates along the crystallographic direction and the wafer breaks into two parts. The surface roughness of the resulting pieces however, strongly depends on the semiconducting material. While GaAs and InP wafers exhibit a straight cutline together with a low surface roughness of the whole cross-section, areas of lower and higher surface roughness make this step unpredictable for Si [51]. Further, the hardness and the hexagonal crystal lattice of certain SiC polytypes make the situation even more complex. From a device perspective this approach is not suitable at all, since a lot of work in terms of device processing and a lot of material can easily get wasted. Therefore more reliable and cost-effective approaches have been investigated that allow for more systematic studies.
The approach taken here for the preparation of smooth surface cross-sections is chemical mechanical polishing (CMP) [52]. This technique consists of several lapping and polishing steps which utilize abrasive particles contained in a polishing slurry that is wetting the sample-lapping plate/polishing pad contact. The chemical component of the slurry that is used for finishing is weakening or breaking bonds on an atomistic level to ensure a high quality surface finish. To avoid a rounding of the sample edges a sandwich structure

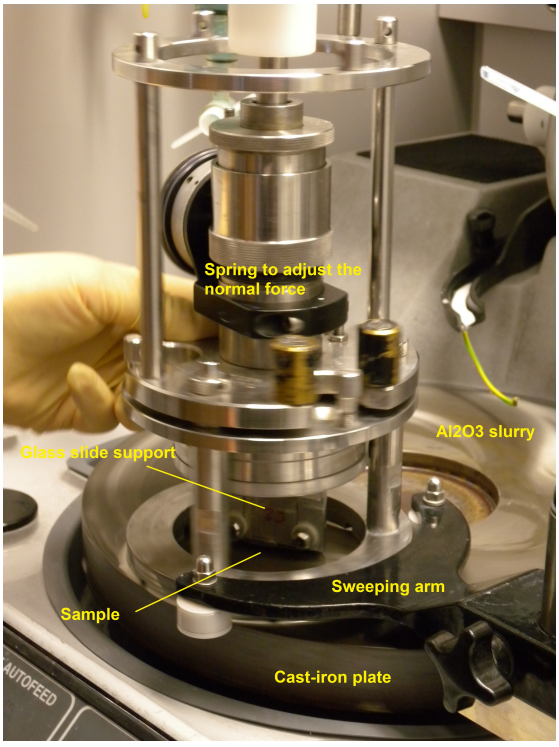

Figure 2.1: The experimental polishing setup consisting of a rotating cast-iron plate for sample grinding, a sweeping arm to ensure a circular motion of the sample and the sample holder. Picture taken by U. Gysin.

consisting of two cleaved device cross-sections that are glued by non-conductive epoxy has been employed. The device active areas were pointing towards the center of this

sandwich. As depicted in Fig. 2.1 an additional glass slide supports the sample inside the chuck. With a spring in the sample holder the normal force can be adjusted. The sweeping arm of the polishing machine causes a circular motion of the sample for a more homogeneous process. The parameter space includes the rotating speed of the cast-iron plate/polishing pad, the amount of polishing slurry used and the normal force. Beside that a fine-tuning with respect to the use of different polishing pads and slurries with varying particle sizes needs to be done for an optimized polishing result.
Due to the different hardness of different semiconducting materials also the polishing process can be entirely different. The parameters that can be changed are discussed within the next lines on the example of Si and 4H-SiC that are the two semiconducting materials used within the scope of this thesis.
For the more advanced Si-technology a standard two-step lapping and polishing process has been developed. Al_2O_3 particles inside the slurry cater for the mechanical material removal of the sample during the grinding step on a rotating cast-iron plate. The subsequent polishing step is conducted on a corklike polishing pad in combination with the Syton SF1 polishing suspension that consists of colloidal silica particles with an average diameter of 250 nm. In a first step the chemical component induces a reaction of surface molecules into soluble complexes that can later on be mechanically removed [53].
SiC is a more challenging semiconducting material in terms of polishing due to its hardness of 9.6 on the Mohs scale which is very close to diamond. Hence, only diamond particles can be used as abrasive materials. In the following table the polishing parameters for a mechanical (MP) and a chemical-mechanical process (CMP) for 4H-SiC are shown: According to Fig. 2.2 the surface roughness for the CMP process is lower

CMP					
Step	Disk	Grain size [μm]	Rot. [rpm]	Weight [g]	Time [min]
Grinding	Cast-iron disk	6	50	300	3
Polishing	Microtex	3	30	400	60
Polishing	Microtex	1	15	400	30
Polishing	Chemcloth	0.25	15	400	15
MP					
Step	Disk	Grain size [μm]	Rot. [rpm]	Weight [g]	Time [min]
Grinding	Cast-iron disk	6	50	300	3
Polishing	Microtex	3	30	400	60
Polishing	Microtex	1	15	400	30
Polishing	MD-Nap	1	15	400	30

Table 2.1: Comparison of a chemical-mechanical and a mechanical polishing process for 4H-SiC in terms of their process parameters. While the first three steps are equal the finishing step for the CMP process is identical to processes used for Si and the MP process is based on a small grain size diamond slurry in combination with a very soft polishing pad.

compared to the MP process. This can be on the one hand attributed to the smaller particle size of the polishing slurry but on the other hand also the action of the colloidal silica on the native oxide of SiC.
For the removal of the residual particles a solvent based cleaning process consisting of multiple Acetone and Isopropanol rinsing and ultrasound steps has been subsequently performed. The final cleaning beforehand the AFM measurements in vacuum was done by an UV-ozone treatment for 60 minutes to remove all remaining organic contaminants.

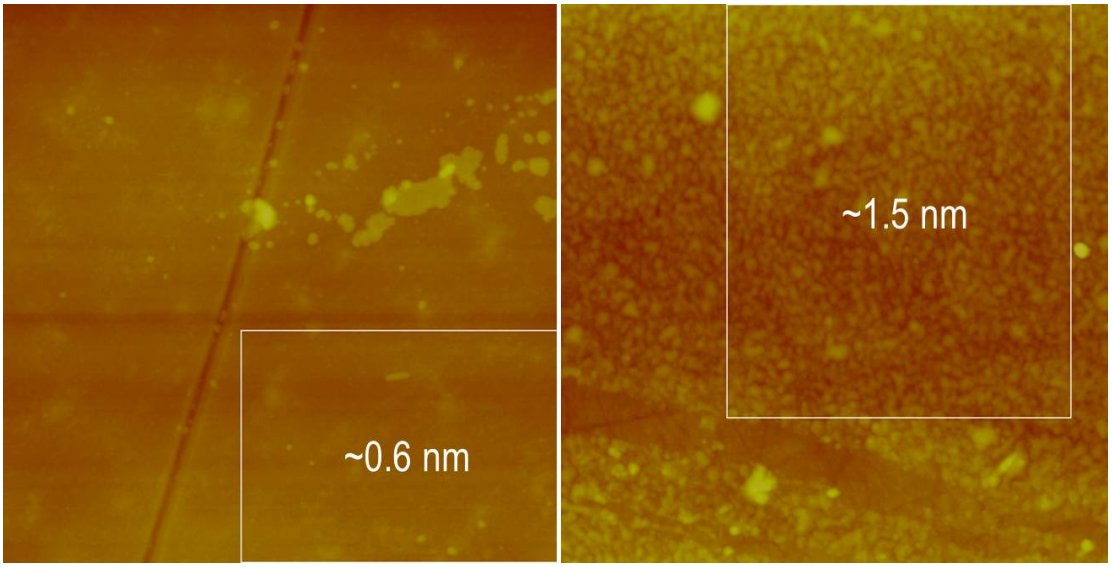

Figure 2.2: Analysis of the surface roughness by AFM under ambient conditions (image size: 2 μm $\times$ 2 μm). The CMP process (left) resulted in a sub-nanometer surface roughness inside the area indicated by the white rectangle. Residual particles increased the roughness of the whole image. The surface roughness value of the MP process (right) was found to be increased.

2.2 SPM-based characterization methods

After the successful cross-section preparation with a surface roughness below 1 nm the sample needs to be contacted from the backside which is done by the sputter-deposition of Aluminum as backside contact. Conductive silver paste is then in a final step used to 'glue' the sample onto the sample holder.
For the assessment of electronically active dopant profiles different SPM based imaging techniques [54] have been implemented in the same experimental system (Fig. 2.3) since so far no single metrology technique has proven to be superior. To rule out artefacts arising from different sample preparation routines or different experimental setups it is crucial that this study is conducted within the same vacuum environment. Further the same calibration structures need to be used to gain a reliable information on the quantification possibilities of each method. While Duhayon et al. [55] gathered first data sets in their pioneering study on dopant profiling, the aim of the research project conducted within this thesis was a more systematic comparison in terms of the quantification possibilities.

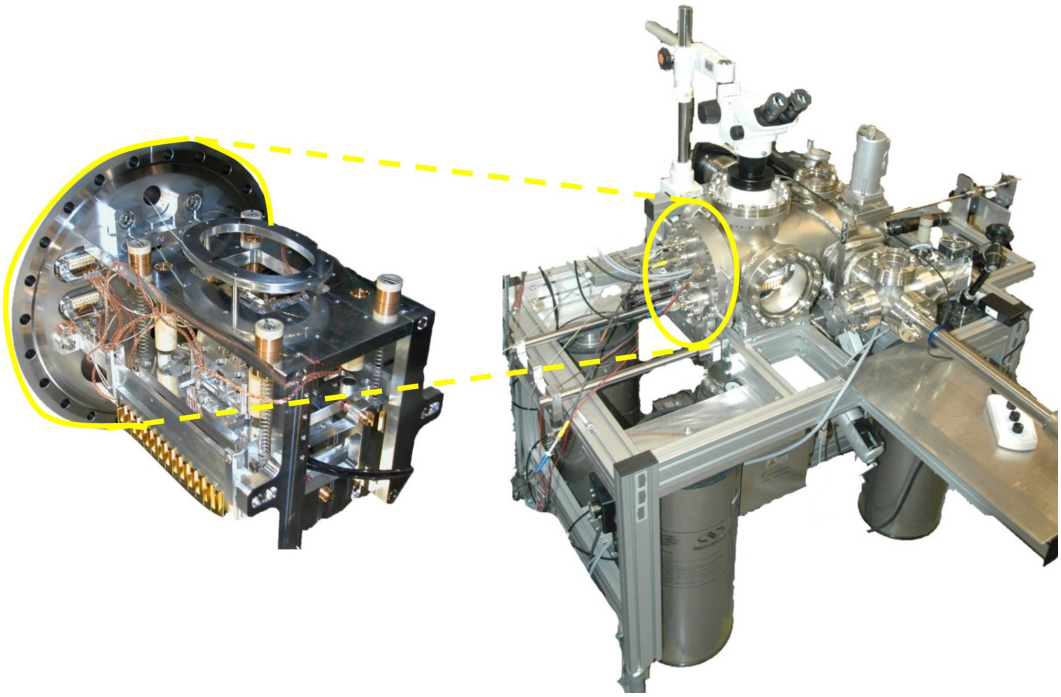

Figure 2.3: The custom-built UHV-SPM system for the dopant profile analysis of power semiconductors is shown. The wide range closed loop scanner with a scan range of 100 μm $\times$ 100 μm $\times$ 25 μm (in x, y and z-direction) even enables the precise scanning of extended Super-Junction structures. Figure taken from [56].

2.2.1 Kelvin Probe Force Microscopy

The principle of the KPFM technique goes back to Lord Kelvin at the end of the 19th century [57]. During his experimental study he was connecting two capacitor plates of different materials so that an electron current from the material with the lower work function towards the material with the higher work function gets established. In the experimental setup used one of the capacitor plates was vibrating at a certain frequency so that the resulting electron current was time dependent. By the application of a DC bias voltage he recognized that the electron current is getting constant, only when the applied bias voltage was exactly matching the contact potential difference between the two metals. KPFM is taking this principle to the nanoscale by replacing one of the plates by a metallic tip [58]. The contact potential difference (CPD) compensation

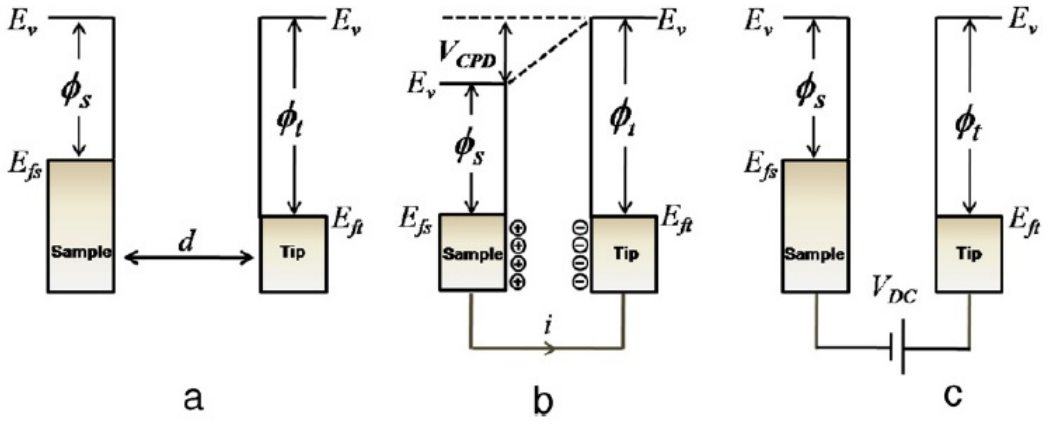

Figure 2.4: The energy level diagram of a metallic tip and the sample under investigation is shown. If there is no connection between the tip and the sample their vacuum levels align (a). Upon connection an electron current that is flowing from the lower towards the higher work function material gets established so that the Fermi levels of the two materials equalize (b). The original situation can be restored by the application of an external bias voltage which has the same magnitude as the contact potential difference (c). Figure taken from [59].

as illustrated in Fig. 2.4 can be understood by considering the tip-sample system as parallel plate capacitor. The electrostatic force of this system is given by $F = -\frac{1}{2}V^2\frac{\partial C}{\partial z}$ and the applied bias voltage is equal to $V = (V_{DC} \pm V_{CPD}) + V_{AC}\sin(\omega t)$ [59]. The sign thereby depends on whether the voltage is applied to the tip (-) or the sample (+). By the combination of these two equations and by the use of addition theorems for trigonometric functions the electrostatic force can be written as sum of the three following terms [59]:

$$F_{DC} = -\frac{\partial C}{\partial z}[\frac{1}{2}(V_{DC} \pm V_{CPD})^2] \tag{2.1}$$

$$F_{\omega} = -\frac{\partial C}{\partial z}(V_{DC} \pm V_{CPD})V_{AC}\sin(\omega t) \tag{2.2}$$

$$F_{2\omega} = \frac{\partial C}{\partial z}\frac{1}{4}V_{AC}^2[\cos(2\omega t) - 1] \tag{2.3}$$

While the first term either gets nullified by the compensation of the contact potential difference, which is defined as $V_{CPD} = \frac{\Phi_{sample} - \Phi_{tip}}{q}$, or results in a static deflection of the cantilever, KPFM utilizes the F_ω component to measure the contact potential difference of the tip-sample system. The $F_{2\omega}$ term can be used for capacitance measurements as will be discussed in the following subsection. The working principle of KPFM is

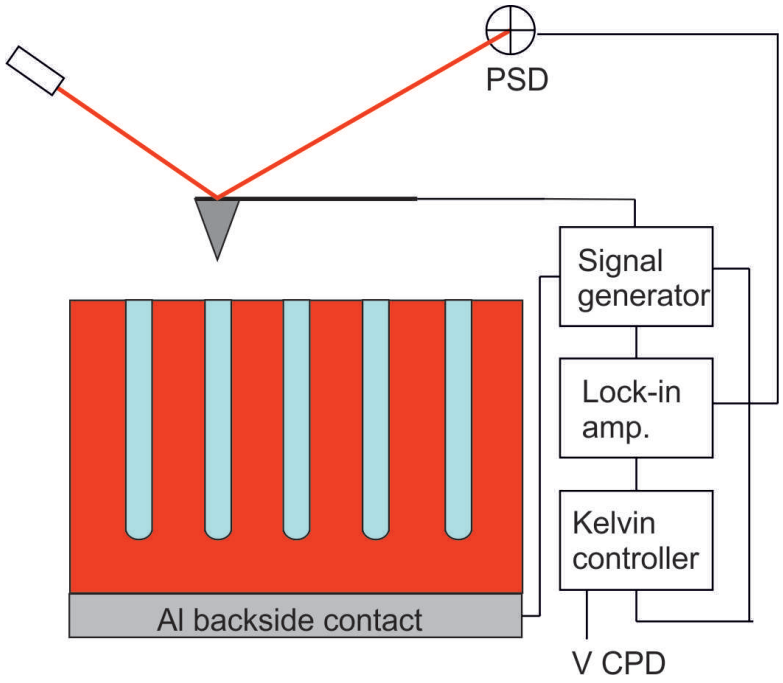

Figure 2.5: A schematic image of the KPFM working principle in terms of their detection and signal processing units is shown. The back contact in this illustration is further extended since otherwise it would be hidden behind the sample cross-section.

depicted in Fig. 2.5 and can be understood in the following way [60]: a signal generator is applying an external bias voltage that consists of an AC component that causes an oscillation of the cantilever at its second eigenfrequency and a DC component that is used to compensate the contact potential difference between the tip and the sample. The second eigenfrequency in this setup is used for the electrostatic force detection while the first eigenfrequency is used for the simultaneous acquisition of the sample topography. Via a lock-in technique the F_ω component can be addressed separately and taken as input for the Kelvin controller which sets the right DC bias to compensate the contact potential difference.

The measured values of the contact potential difference of the tip and the sample can be used to exploit the relative and absolute quantification potential of this method. Both methods depend on the formula for the concentration of acceptor (donor) atoms which

is given by

$$N_A = N_V \exp\left(-\frac{E_F^{sample} - E_V}{k_B T}\right) \tag{2.4}$$

where N_A is the acceptor concentration, N_V is the density of valence band states, E_F^{sample} is the Fermi energy of the sample, E_V is the valence band energy, k_B is the Boltzmann constant and T the temperature according to [61]. In the following, the equations will be derived for p-type structures since the regions of interest in our samples are p-type. By

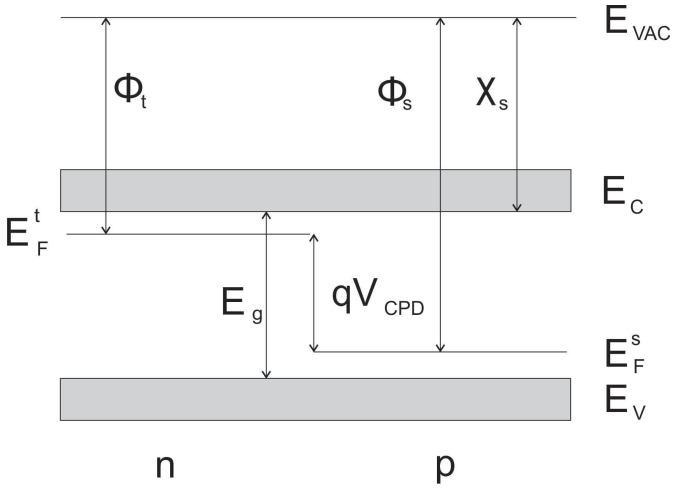

Figure 2.6: Energy level diagram for a p-doped sample and an n-type tip to illustrate the contact potential difference.

expressing the numerator in terms of the CPD and the material constants of the sample (see Fig. 2.6) and building the difference between a well characterized calibration layer and an unknown region in terms of the dopant concentration one can derive the following equation

$$\Delta V_{CPD} = \frac{k_B T}{q} \ln\left(\frac{N_A^1}{N_A^2}\right) \tag{2.5}$$

that allows for the determination of the dopant concentration in a relative way. In the same manner in principle also an absolute quantification (see Eq. 2.6) should be possible if the work function of the tip is well-known. Adsorbates and defects at the surface however compromise these quantification possibilities.

$$N_A = \frac{N_V}{\exp\left(\frac{\Phi_t - \chi_s - E_g + eV_{CPD}}{k_B T}\right)} \tag{2.6}$$

2.2.2 Scanning Capacitance Force Microscopy

The second method which has been investigated is SCFM which utilizes the $F_{2\omega}$ component according to Eq. 2.3 of the electrostatic force that develops when an external

bias voltage is applied between the tip and the sample. Further, in Ref. [62] it was found that on semiconducting samples the capacitance gradient not only depends on the sample topography but rather also on the applied bias voltage. Therefore $\frac{\partial C(z)}{\partial z}$ can be split into the sum of a DC and an AC component:

$$\frac{\partial C(V,z)}{\partial z} = \frac{\partial C(V_{DC},z)}{\partial z} + \frac{\partial^2 C(V_{DC},z)}{\partial V \partial z} V_{AC}\cos(3\omega t) \tag{2.7}$$

This approach can be understood by considering a capacitance system that consists of an oxide capacitance and a variable series capacitance of the depletion layer. The modulating AC voltage therefore alters the depletion layer capacitance.
By inserting the last term of this equation into Eq. 2.3 a component with three times the original oscillation frequency appears:

$$F_{3\omega} = \frac{1}{8}\frac{\partial^2 C(V_{DC},z)}{\partial V \partial z} V_{AC}^3 \cos(3\omega t) \tag{2.8}$$

The operating principle is similar to the one used for KPFM, however different electronic components cater for the readout of the $\frac{\partial C}{\partial V}$ signal. Analogously to KPFM the first cantilever eigenfrequecny is used for the detection of the topography signal [63]. The

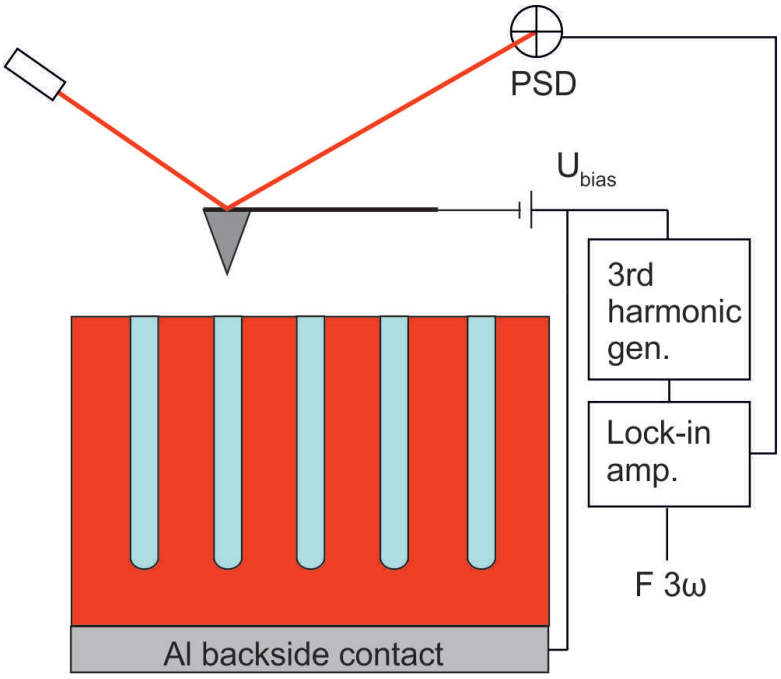

Figure 2.7: A schematic image of the dynamic mode SCFM working principle in terms of their detection and signal processing units is shown. The back contact in this illustration is further extended since otherwise it would be hidden behind the sample cross-section.

frequency of the AC bias voltage component is thereby chosen in such a way that it equals $\frac{1}{3}$ of the second cantilever eigenfrequency. In this way the resonance enhanced detection

principle can be exploited. A frequency converter is generating the third harmonic of this AC bias as input signal of the lock-in amplifier so that the right component of the electrostatic force signal can be selected for mapping the $F_{3\omega}$ signal. Notably, the depletion width is larger the smaller the doping concentration is. Hence, the change of the total capacitance is larger in the low dopant concentration regime. Bias spectroscopy measurements have confirmed this trend, however the shape of these curves is not yet well understood so that dopant profiling in a quantitative manner is still not possible. Technology Computer Aided Design (TCAD) simulations on this issue are ongoing [64] so that the potential of this method can be addressed in future work.

2.2.3 Scanning Spreading Resistance Microscopy

The last method to be discussed here in the comparison of SPM-based methods for the quantification of electronically active dopant profiles is SSRM [65]. It differs from the aforementioned methods in its contact mode operation. The technique as such is a miniaturization of the Spreading Resistance Probe (SRP) principle [66] that uses two micrometer sized probes instead of an AFM tip with typical tip diameters below 100 nm.
A characteristic of this technique is the high normal force (in the range of μN) that needs to be applied to the sample surface to ensure that the spreading resistance is the dominant resistance contribution and that the total resistance can be approximated by it. The rather large cross-sectional area of power devices as well as of the probe is leading to only small additional contributions to the total resistance so that this approach [67] is valid for the samples discussed within the scope of this thesis. The second effect of the high pressure is a phase transformation of a tiny sample volume just below the tip from a less conducting to high conducting state. The electrical radius a of this pocket is even smaller than the tip radius which explains the high resolution of this technique. The Maxwell spreading resistance formula [68]

$$R_{spr} = \frac{\rho_{sample}}{4a} \tag{2.9}$$

where ρ_{sample} is the resistivity of the sample and a is the electrical radius, depends on the dopant concentration n/p via the resistivity of the sample.

$$\rho_{sample} = \frac{1}{q(n\mu_n + p\mu_p)} \tag{2.10}$$

For p-type semiconductors $n = 0$ and the formula can be simplified so that it contains only the charge of the carriers p, their concentration and their mobility μ_p. Together with Ohm's law the measured current can be expressed as a function of the hole concentration

is given by

$$I = 4aeUp\mu_p \tag{2.11}$$

whereas U is a DC bias voltage that is applied between the tip and the sample back-contact. The topography is monitored by a beam deflection setup while the dopant

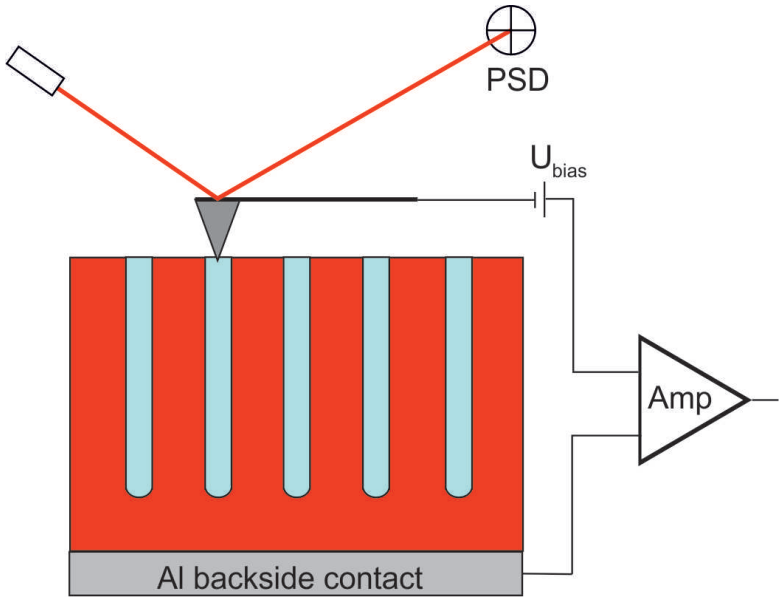

Figure 2.8: A schematic image of the SSRM working principle in terms of their detection and signal processing units is shown. The back contact in this illustration is further extended since otherwise it would be hidden behind the sample cross-section.

dependent current is the output signal of a logarithmic amplifier. Even tough this principle seems to be quite straightforward numerous deviations from this ideal situation make the quantification more complex. For instance, the carrier mobility depends on the dopant concentration itself and on the sample temperature. While the latter has not a big influence, the change of the carrier mobility for intermediate concentrations in the order $N_A = 10^{17}$ cm^{-3} is quite significant [34]. Further, the nature of the nano-contact between the tip and the sample is not ohmic but shows Schottky-like features in spectroscopic measurements. All of these examples are topics of current research and will be discussed later on in Chapter 3.

Due to this non-idealities a calibration procedure was up to now based on the use of well-characterized staircase samples [69] with a varying dopant concentration. By comparing the resistivity profiles of this reference conclusions on the dopant concentration of an unknown sample can be drawn. The strength of this method - as demonstrated by Eyben et al. [70] - lies in the high degree of reproducibility. The abrasive action of the tip while scanning the sample in contact mode leads to a self-preparation of the surface. Therefore SSRM is less sensitive to preparation induced defects as the two non-contact methods discussed before.

2.3 Trench MOSFET fabrication and mobility measurements

The second part of this methodological introduction is dedicated to the fabrication of nanoscale trench MOSFETs in 4H-SiC. Therefore a dry etching process with the aim of fabricating trenches of 3 μm in depth and widths ranging from 0.5 μm to 3 μm had been developed. The establishment of a highly controllable and reliable etching process is crucial for further device processing and a successful integration of nano and micro-trenches can be used as platform for different device architectures such as MOSFETs or MOS-Capacitors. In Fig. 2.9a-d the main fabrication steps towards a trench MOSFET

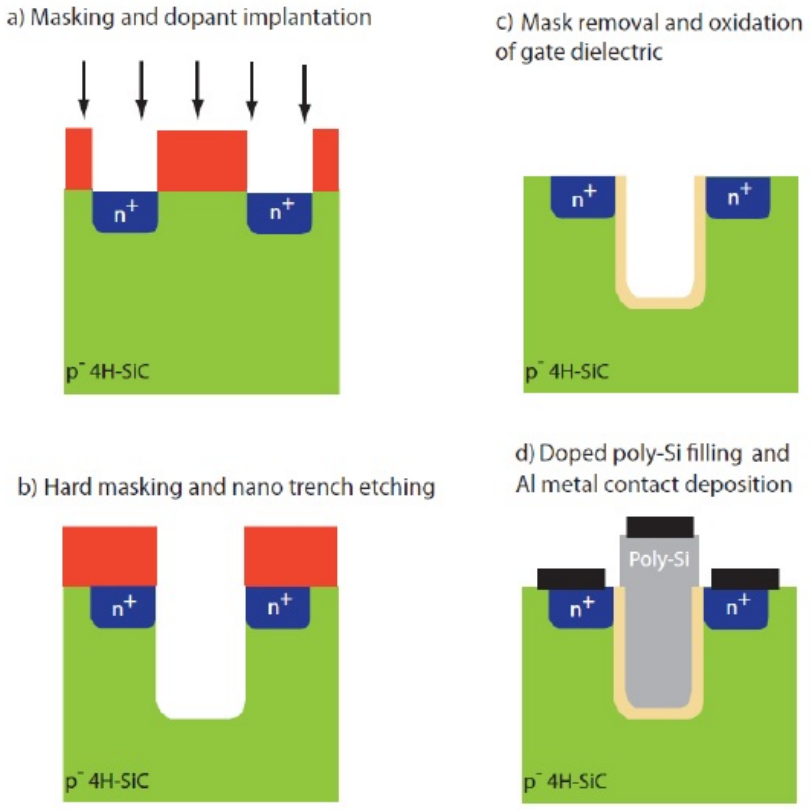

Figure 2.9: The main fabrication steps towards a working MOSFET are shown. The dopant implantation and activation (a) is followed by a trench etching process (b). Afterwards the U-shaped trench can be oxidized and filled with a doped polycrystalline Si gate. In a last step metal contacts that show an ohmic behaviour need to be deposited (d). Figure adapted from [71].

are shown. Main focus in this section will be given to the dry etching process since it had been developed at LMN. Further, the main processing steps and the remaining challenges of the full fabrication process flow will be briefly discussed to gain a better insight on the device manufacturing. In the last subsection of this chapter the electrical characterization technique for mapping the mobility inside the thin conducting channel will be discussed.

2.3.1 Ion implantation

The first step in the process flow towards a working trench MOSFET is the realization of the targeted dopant architecture. The impurity type of the source and drain regions as well as of the substrate determine the type of the transistor. Within this project an n-channel transistor had been designed. Therefore, donor impurities need to be incorporated into the p-doped substrate. As shown in Fig. 2.9a the method of choice for SiC is ion implantation since the dopant atoms suffer from very low diffusion coefficients. This is on the hand beneficial for the design of shallow junctions but on the other hand a selective dopant process by diffusion is not feasible. In Si technology however, ion implantation also almost completely replaced thermal diffusion processes due to the better lateral confinement of impurity atoms [52].
Due to the missing availability of an ion implantation source at PSI the implantation process had been outsourced to a subcontractor who performed the dopant profile simulations and also the did implantation of Phosphorous atoms to form n^+ wells in the p-doped substrate. Further, also n-type substrates with highly Aluminum doped source and drain regions have been investigated.
For the implantation process itself dopant atoms that are primarily in a gaseous state need to be ionized and extracted from the ion source so that they can be later on filtered according to their mass. After passing through an acceleration tube the ion beam is spread over the whole wafer by an appropriate electromagnetic lens system. Inside the wafer the ions are stopped by numerous, stochastic nuclear and electron stopping processes [72]. Therefore simulations on the implantation process are required to predict the right processing parameters. Within this project the ion energy needed to be chosen in such a way that a 200 nm deep box profile is accomplished. As shown in Fig. 2.10 the targeted depth profile of the implantation could be reached by an implantation energy of 20 keV. Notably, for SiC the implantation process has to be performed at elevated temperatures to avoid an amorphization of the substrate [41]. Hence, a temperature of 500 °C had been chosen to limit the damage to the crystal lattice. During the subsequent high temperature dopant activation step the remaining irregularities of the crystal lattice almost completely vanish so that the crystalline nature gets restored without changing the polytype during this processing sequence.

2.3.2 Inductively coupled plasma reactive ion etching of trenches

The patterning of the trench structures was done by electron beam lithography [52]. In a first step a 100 nm thick Cr hard mask was deposited on top of the wafer. After spincoating a Polymethylmethacrylat (PMMA) layer on top, an electron beam was used to break the bonds of the resist at the positions where the trenches later on should be etched. The selective opening of the hard mask was then obtained by a Cl_2 based

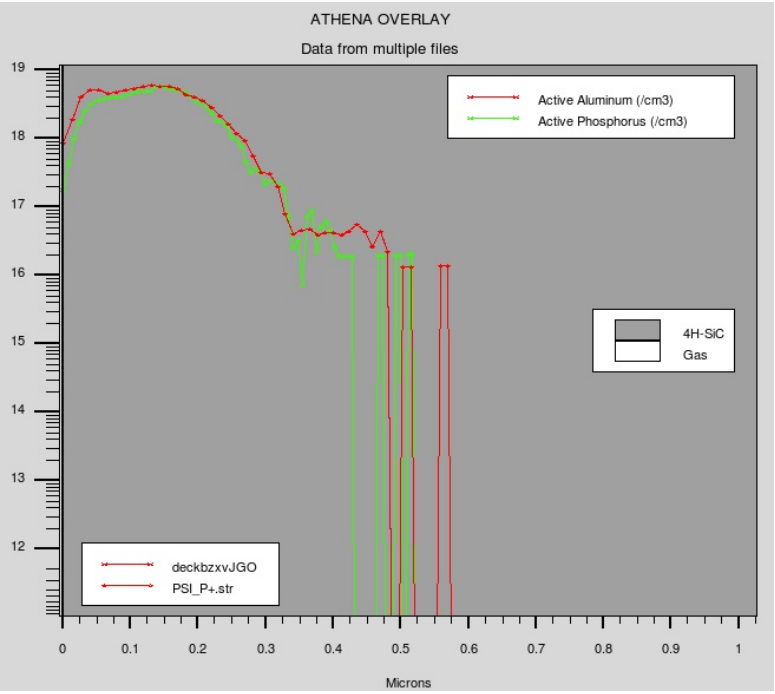

Figure 2.10: Simulated dopant profiles provided by Ion Beam Services are shown for phosphorous and aluminum as n and p-type dopant atoms respectively. A box profile with a depth of 200 nm had been realized with an implantation energy of 20 keV and an implantation angle of 0 degrees. Simulations performed by Ion Beam Services.

reactive ion etching (RIE) process. Chromium had been chosen as hard mask material since photoresist or silicon dioxide are not suitable for etching deep trenches into 4H-SiC due to their limited selectivity. The shape after the etching process was monitored by our in-house SEM.

The etching mechanism of RIE systems consists of two components, namely a physical and a chemical component [52]. The first leads to a mechanical removal of the target material by the impinging ions as for example in an ion milling process. The chemical component comes into play by the gases that are used to create the plasma. They are chosen in such a way that they can react with the surface atoms or molecules of the substrate to form a more volatile species that can be easily removed.

Within the experimental work of this thesis an Oxford plasma lab RIE system that is equipped with an inductively coupled plasma (ICP) head had been used. The plasma thereby gets generated by a radio-frequency (RF) source which creates a time varying magnetic field. As a consequence an electric field gets induced inside the plasma chamber. Due to the different masses of the electrons and ions contained inside the plasma, the fast response of the electrons to the varying electric field causes further ionizations of gas molecules [73]. The forward power creates a DC bias between the charge neutral plasma and the electrode where the sample is mounted, so that vertical ion flux towards the sample gets established. With the geometry as shown in Fig. 2.11 the plasma

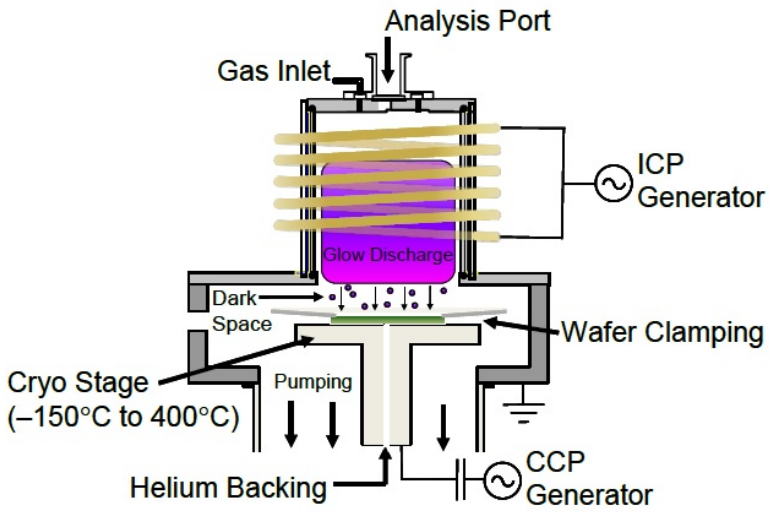

Figure 2.11: Schematical illustration of an RIE system with an inductively coupled plasma head and a capacitively coupled forward power. Image taken from [73].

density and the directional forward power which accelerates the ions towards the surface get decoupled. Hence, high density plasmas can be generated that cause a very soft material removal by the physical etching component.

As a starting point regarding the plasma chemistry an SF_6/O_2 gas mixture had been used, since in previous studies high etching rates with this process had been realized [74]. Chemical reactions of SF_6/O_2 with SiC form volatile SiF_x and CF_x complexes while the addition of O_2 is leading to different pathways for the Carbon removal in terms of CO, CO_2 and COF_2. Hence, also the etching rate gets increased with the oxygen content up to an amount of 20% O_2.

Beside the plasma composition there are various other parameters that can be tuned to get an optimal etching result. To gain a better understanding of the processes itself and the crucial processing parameters an initial starting recipe that has been suggested by the manufacturer of our etching equipment had been used. Thereafter, process parameters have been adjusted according to published articles and the experimental results from etching experiments at the LMN cleanroom facility at PSI.

In the following table the evolution of the etching parameters is shown: The initial experiment, as shown in Fig. 2.12a, resulted in a pronounced microtrenching effect at the trench corners. In a fist step this recipe had been adapted according to the study by Biscarrat et al. [75] where they have found that a higher ICP power can diminish the microtrenching effects. Therefore the ICP power had been manually ramped up in consecutive steps to reach a higher plasma density in the end. The ramping is beneficial since the ignition of the plasma at lower powers is more stable. As depicted in Fig. 2.12b the microtrenching effect could be diminished, however the present shape was still

Process	I	II	III	IV
SF_6 flow [sccm]	10	10	10	10
O_2 flow [sccm]	2	2	0	0
Ar flow [sccm]	0	0	0	2
Pressure [mTorr]	10	10	8	10
RF power [W]	30	30	7	11
ICP power [W]	500	1000	1000	1000
V_{DC} [V]	115	70	11	10
Time [min]	20	15	20	20
Etching rate [nm/min]	155	165	80	65

Table 2.2: Comparison of etching parameters for different processes. Process I refers to the initial starting recipe from Oxford instruments. Processes II, III and IV have been improved according to published articles and the acquired experimental results.

not satisfactory since these edges would cause a crowding of the electric field during the device operation and would therefore lead to a premature breakdown of the device.
An other suggestion, namely to reduce the DC bias voltage to a value around 10 V, came from our industrial collaborator ABB. At the same time also the plasma chemistry was changed since it has been found for 6H-SiC [76] that the O_2 fraction can cause the formation of a SiF_xO_y that is more easily charged than the SiC substrate. Hence more ions will be deflected towards the trench corners. Even tough the pressure for process III was slightly lower than for process IV (see table 2.2) the obtained trench profile 2.13a showed a higher degree of isotropy. Therefore it can be concluded that the effect of the pressure did not lead to the superior trench shape in Fig. 2.13b. Whether the microtrenching could be eliminated by the smaller DC bias or by the omission of O_2 is still under investigation. Also a combination of both effects is plausible.

2.3.3 Oxidation process

One of the unique properties of SiC - that has also driven the material development in terms of power semiconductor applications - is that a SiO_2 layer can be thermally grown. As mentioned in Chapter 1 the passivating nature of SiO_2 on dangling bonds of the Si crystal was one major breakthroughs in Si technology. In SiC however, the presence of C atoms makes the situation more complex and the origin of the reduced carrier mobility at the SiO_2/SiC interface is not yet fully understood.
To take the presence of C atoms during the thermal oxidation process into account the Deal Grove model for Si [77]

$$d_{ox} + Ad_{ox}^2 = Bt \tag{2.12}$$

where d_{ox} is the oxide thickness, t is the oxidation time and B and $\frac{B}{A}$ are the parabolic and linear rate constants, has been extended by considering the out-diffusion of product

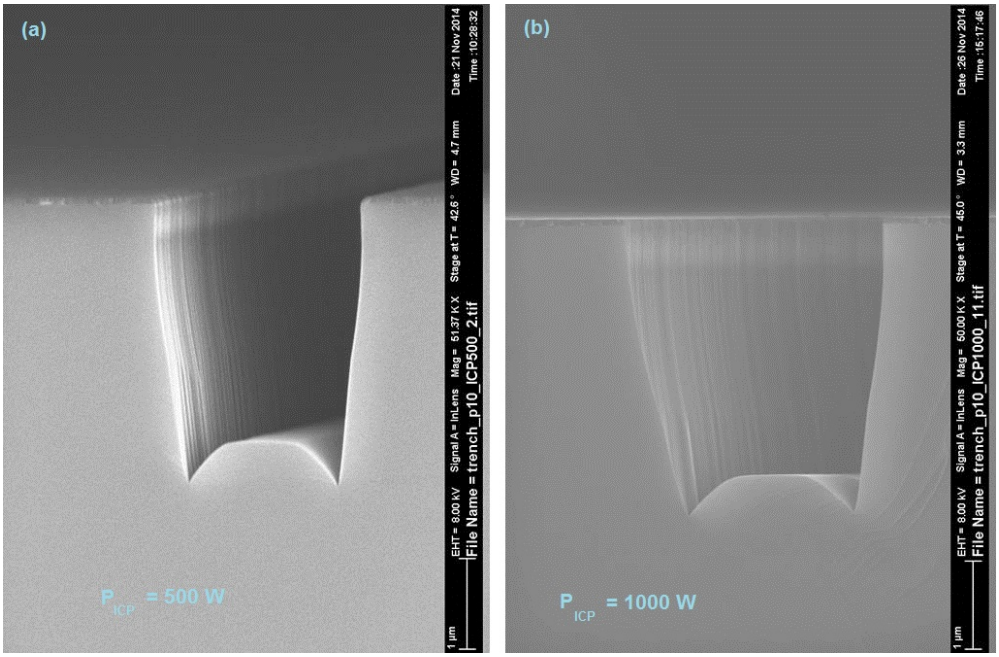

Figure 2.12: The initial recipe (process I) resulted in pronounced microtrenching effects at the trench corners (a). An increased ICP power (process II) could slightly diminish this effect (b).

gases such as CO and their removal from the oxide surface [78]. For thin oxides the oxidation rate is showing a linear dependence on the oxidation rate while for thicker oxides a parabolic relationship is observed. The silicon and carbon emission model suggests that the initial oxidation rate is suppressed by the accumulation of Si and C atoms near the interface [79].

Furthermore the oxidation rate depends critically on the temperature of the oxidation furnace where the wafer gets in contact with the oxidizing agent. For SiC oxidation temperatures are typically above 1050 °C [41]. Notably, the character of the thermal oxidation is anisotropic and has to be considered for an appropriate device design.

In contrast to Si, SiC is showing a much higher density of interface trap states [80] that can not be easily passivated by hydrogen annealing. As a consequence charge carriers can get trapped and the mobility inside the channel is significantly reduced. Therefore, the device performance of current MOSFETs is still limited. Different strategies to overcome this limitation have been proposed and post oxidation annealing treatments in phosphourous or nitrogen ambients resulted in a desired passivating effect and therefore in increased channel mobilities [81]. The technologically most advanced processes use a nitridation of the SiO_2/SiC interface either by post oxidation annealing treatment under NO or N_2O ambients or by the addition of N_2O during the oxidation process itself. With this technique it has been demonstrated that the channel mobilities can be increased by at least a factor of three, depending on the utilized crystal facet [82].

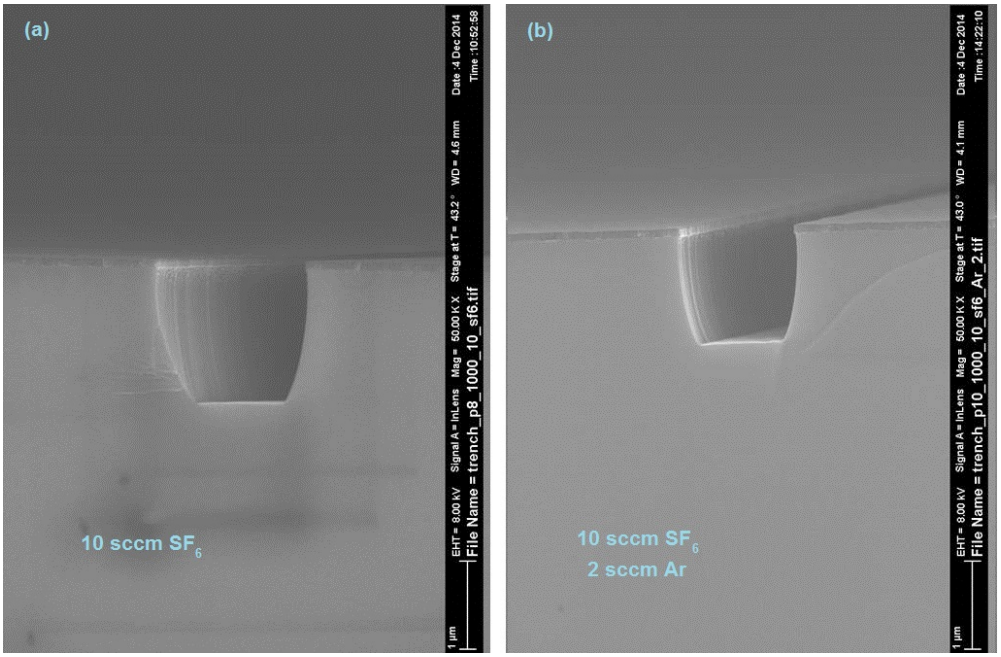

Figure 2.13: The advanced recipes (process III (a) and IV (b)) showed a microtrenching free trench shape after the etching process. The two different processes differ however in their sidewall steepness. While process III (a) was not able to etch vertical sidewalls the sidewall angle of process IV was sufficient for the fabrication of devices.

2.3.4 Polycrystalline Si filling and metal contacts

The last step regarding the fabrication of a trench MOSFET includes the contacting of the source, drain and gate electrodes. For the gate stack usually a doped poly-Si is used to fill up the trench instead of a direct metal deposition due to its superior thermal properties. The poly-Si gate can withstand the high processing temperatures of SiC technology and has a well-established process library. For the contacts to the source and drain area of the device it is important that they show an ohmic behaviour since otherwise the increased contact resistance would lead to higher losses in the ON-state of the device. For *n*-type 4H-SiC typically Ni contacts are deposited and later annealed to form Ni_2S [83]. The in this way adjusted barrier height together with the high underlying dopant concentration ensure a narrow Schottky barrier so that electron tunnelling can occur. Further studies on this topic also investigated the formation of a graphite layer at the interface with the conclusion that this formation is not the main reason for the observed ohmic behaviour [84].

2.3.5 Assessment of channel mobilities

The effective mobility of an n-channel MOS-controlled FET is given by

$$\mu_{eff} = \frac{g_d L}{W Q_n} \tag{2.13}$$

where L is the channel length, W is the channel width, Q_n is the mobile channel charge density and g_d is the drain conductance which is defined as the change of the drain current with respect to the drain-source voltage when the gate-source voltage is kept constant [85]:

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \tag{2.14}$$

The mobile channel charge density needs to be determined in the following way: in a first step the capacitance of the source and drain region is measured in the accumulation regime. Since under these conditions no channel is formed, only the two overlap capacitances of the drain and source regions are measured when the substrate is grounded. In a second step, at a sufficiently high gate voltage, an inversion layer is formed and therefore also the channel capacitance contributes to the overall capacitance signal. From the difference of these two capacitance values conclusions on the mobile channel charge can be drawn. The drain conductance can be extracted from the slope of the drain output characteristics. Together with the geometrical parameters of the channel, the effective channel mobility can be evaluated using Eq. 2.13.

CHAPTER 3

Low dopant regime carrier profiling by SPM methods

Within this chapter the answer to the question if there is any SPM based method that can quantitatively map carrier concentrations with a high sensitivity shall be given. For the evaluation, the three most promising techniques, namely Kelvin Probe Force Microscopy (KPFM), Scanning Capacitance Force Microscopy (SCFM) and Scanning Spreading Resistance Microscopy (SSRM) have been implemented in the same, custom-built vacuum system. To gain meaningful results special test structures with a very low dopant concentration have been manufactured and assessed with the aforementioned methods. Even though some of them may look on the first sight quite similar, the underlying physical contrast mechanism is different and leads to significant differences in terms of their resolution. After discussing strengths and weaknesses of each method, in the second part of this chapter a detailed analysis of the quantification potential of most superior technique SSRM, will be given. It will be shown that there are several ways to determine the carrier concentration profile. Among them, different principles either based on the depletion width or on the underlying carrier mobility are discussed.

3.1 Quantitative analysis of ultra-lightly doped Si Super-Junction structures by complementary two-dimensional carrier profiling techniques implemented in a Scanning Probe Microscope

It is well known that the device functionality and performance of semiconductor devices strongly depend on the dopant profile architecture [61]. Thus, a precise control of the dopant implantation and diffusion processes during fabrication as well as profound knowledge about the dopant profile evolution during the whole product life cycle is essential for the manufacturing of reliable high-performance semiconductor devices. A broad range of dopant profiling techniques has been developed [86] and tested or used for device manufacturing [87]. The following important characteristics for a dopant profiling technique have been identified: (1) high spatial resolution, (2) good reproducibility, (3) high sensitivity and (4) the ability to quantify dopant concentrations. Notably some techniques, like Secondary Ion Mass Spectrometry (SIMS) destructively analyse the three dimensional distribution of dopants while other techniques depend on the also destructive preparation of a surface cross-section of the 'to be investigated' device. De Wolf et al. [88] highlighted the potential of Scanning Probe Microscopy (SPM) based methods for simultaneously accomplishing all these demands while well-established, former industry standard techniques such as Secondary Ion Mass Spectroscopy (SIMS) [89] and Spreading Resistance Probe (SRP) [66] are of limited practical use. SPM-derived techniques evolved far from the initial capability for topographic surface mapping to a pool of versatile experimental techniques revealing dopant contrast [55] by means of capacitance [90], resistance [65] and surface potential [58] imaging down to the atomic and molecular scale. Nevertheless, due to the irregular preparation routines of sample cross-sections as well as due to the use of different experimental setups used for previous measurements [55] a comparison of SPM techniques in their capability for doping quantification has so far not been performed. Importantly in the context of power semiconductors, such a comparison should critically address the sensitivity as well as the ability to quantify dopant concentrations over the full dynamic range in all, also the most advanced devices. This is of utmost importance since either lightly doped drift layers [91] in wide band gap devices with concentrations starting from as low as 10^{14} cm^{-3} or precisely charge compensated pillars [92] in Super-Junction [93] devices are utilized to block high voltages when the device is operated in reverse direction.

3.1.1 Super-Junction device architecture

The samples that are investigated within this comparison are similar to a conventional Si SJ-MOSFET with its characteristic pillar structure but differ in the surface-near regions

of the active device area. This is due to the fact that a reference dopant concentration to gauge the measured SPM signals is needed. At a first stage, resistivity measurements have been performed on the subsequently grown calibration layers to serve as reference points for the calibration procedure. These calibration layers and measurements provide a superior alternative to the fabrication and analysis of separate staircase calibration samples [69]. As shown in Fig. 3.1, beside the calibration structures on top the charge-

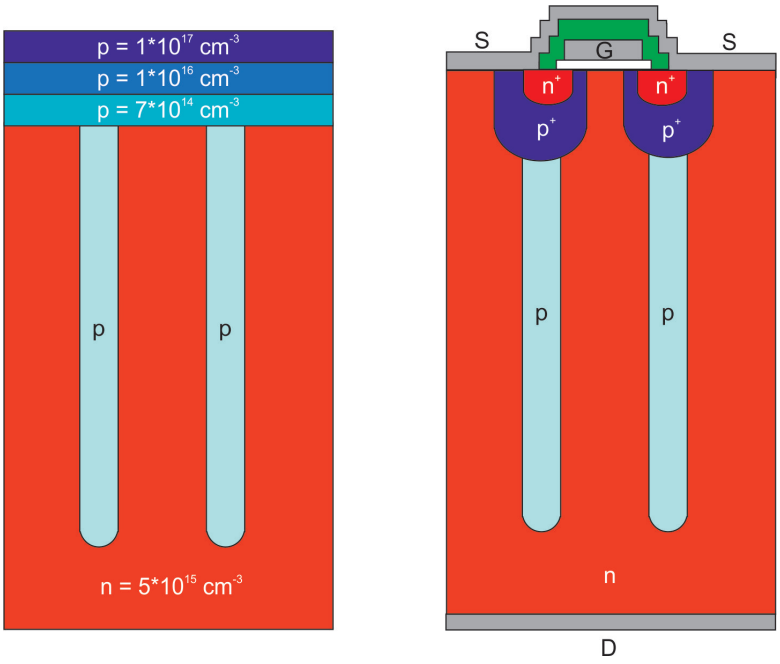

Figure 3.1: (a) Schematic representation of the geometry and the 'as grown' dopant profile of the Super-Junction test samples and the p-doped calibration layers (dark blue) and trenches (cyan), embedded in a n-doped substrate (red). (b) Device architecture of and dopant distribution within a vertical Super-Junction MOSFET device with its three terminals, gate (G), Source (S) and Drain (D). Alternating p and n doped pillars cater for charge compensation in blocking mode while exploiting the potential of one carrier type in forward operation.

compensated pillar structure, which is shaping the horizontal component of the electric field E towards an increased breakdown voltage of this vertical device, is kept in the same way as compared to vertical power MOSFETs. Thereby, the breakdown performance can be tuned beyond the silicon limit [49]. The manufacturing of such pillar structures is done by a trench etch and epitaxial refill process. Details on the process flow and the process parameters can be found elsewehre [94].

3.1.2 In-depth comparison

In the present work, three SPM-based methods, namely Scanning Capacitance Force Microscopy (SCFM) [62], Kelvin Probe Force Microscopy (KPFM) [58] and Scanning Spreading Resistance Microscopy (SSRM) [65], which are capable for the determination

of carrier profiles, *i.e.* electronically active dopant profiles, at low concentrations have been selected and incorporated in the same measurement system for an in-depth comparison. Importantly also, to rule out artefacts originating from the sample preparation procedure, the same scheme has been employed in the preparation of the specimens probed by all three methods. The specific scheme has been defined consequent to the examination of several different preparation approaches for the sample cross-section. We found that the chemical mechanical polishing (CMP) process achieved the best results in terms of a low surface roughness (below 1 nm, as shown in fig. 3.2a) and resulted in a low density of surface states. The latter is needed to avoid the pinning of the Fermi levels of the probing sensor-tip and the sample and is most important to allow for quantitative Contact Potential Difference (CPD) measurements representing the 3D (bulk, *i.e.* not surface modified) properties of the material below the surface cross-section. The topographic images, like the one shown in Fig. 3.2a were acquired simultaneously

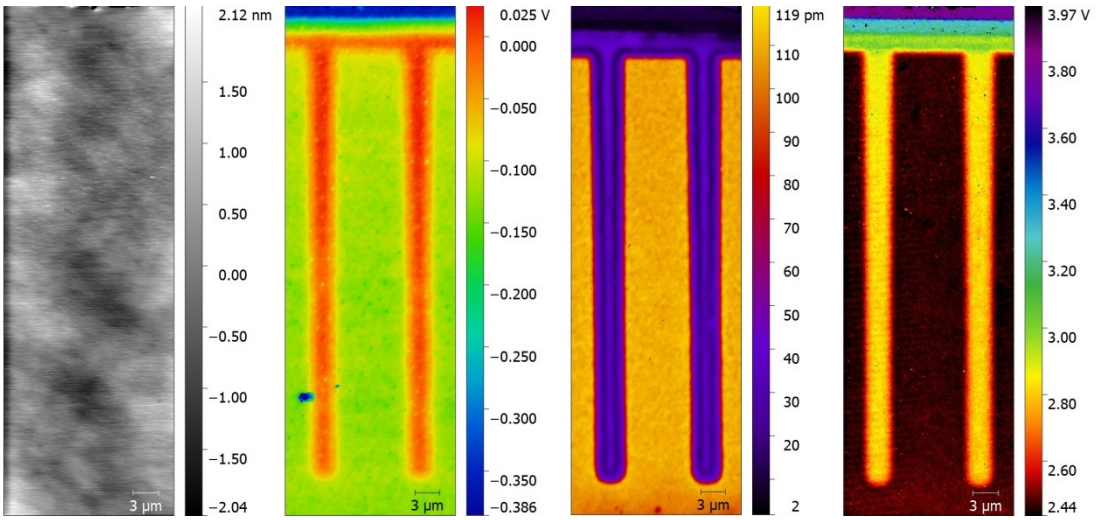

Figure 3.2: (a) Simultaneously acquired topographic images while either KPFM (b) or SCFM (c) measurements were performed by the oscillation of the second eigenmode. (c) As the surface is modified by measurements in contact mode, SSRM measurements (d) were always performed at the end of each measurement sequence and on each specimen. Figure adapted from unpublished AFM data by U. Gysin.

to the corresponding dopant map. SSRM, unlike the other, non-contact force detecting microscopy techniques, involves scanning the specimen in contact mode while the latter detect forces by measuring the modification of a higher harmonic of the cantilever resonance frequency in general and also when applied for dopant profiling [95]. As can be seen in Fig. 3.2a, there are no topographic features visible in either dopant imaging technique which correspond to the faintly visible features in the topography channel. It is therefore concluded that the sample preparation as established is successful in producing sufficiently flat specimens and the nature of the physical contrast (Fig. 3.2b-d) is attributed to a pure dopant effect. The analysis of the sensitivity of each method and

comparison to the theory is complex since there are a variety of effects which complicate quantitative dopant profiling. Starting with KPFM, the lowest p dopant concentration difference of the first two calibration layers is exactly one order of magnitude (see Fig. 3.1a). According to the formula for the CPD difference between two layers,

$$\Delta V_{CDP}^{1-2} = \frac{k_B T}{q} \ln \frac{N_A^1}{N_A^2} \tag{3.1}$$

where k_B is the Boltzmann constant, T is the temperature, q is the elementary charge and $N_A^{1,2}$ are the acceptor densities, two plateaus should be visible in the dopant map with 60 mV height difference at room temperature. Since the calibration layers could be clearly resolved (see Fig. 3.2c) it can be considered that the resolution for dopant detection and quantification is below this value. While this method can only be utilized for relative dopant profiling of differently doped areas, KPFM in principle also provides a tool to directly quantify concentration values if the work function of the tip is well known. However, the corresponding formula is not generally applicable due to the strong influence of defect states on the band structure. Even experiments performed under defect passivating laser illumination conditions have shown that the conduction and valence bands are bent towards each other, therefore resulting in an underestimated built-in voltage across the *pn* junction.

The theoretical relative value of 127 mV for the CPD between the two outmost calibration layers is not in good agreement with the experimental values of 332 mV. This is attributed to the high surface sensitivity of a few nanometers of the Kelvin probe method, which pronounces features at the surface like the presence of oxide layers, adsorbates or defects and the surface carrier density which is prone to modifications by dopant depletion. The 'surface bias' of KPFM relates to the non-contact measurement where the average tip-sample separation is comparable to the information depth. While also comprising a non-contact SPM technique SCFM operates in a different cantilever frequency range and utilizes a very different physical quantity utilized for mapping the dopant concentration. The working principle of SCFM is similar to Scanning Capacitance Microscopy (SCM) [96] with the difference that the capacitive response to an external electric stimulus is detected via the interaction force which is modifying the cantilever oscillation and not electrically as it is the case for SCM [97]. The read out of the amplitude and phase signal from SCFM measurements which can be related to the dopant concentration is carried out by a lock-in amplifier that is able to separately address the 3ω component of the electrostatic force [62]. It is interesting to note that the change of the depletion layer capacitance signal with respect to an AC bias voltage is larger for smaller doping concentrations. This characteristic makes this method an ideal candidate for the investigation of power devices with their lightly doped drift layers. For SCFM the information depth can be estimated by the maximal depletion layer width

[34]

$$W_{D,max} = \sqrt{\frac{4\epsilon_s kT \ln(\frac{N_A}{n_i})}{q^2 N_A}} \tag{3.2}$$

where ϵ_s is the permittivity of the semiconductor and n_i is the intrinsic carrier density. The information depth, in contrast to KPFM, is much larger and critically depends on the dopant concentration. The corresponding maximum depletion layer widths of the three calibration layers used in this study starting from the topmost layer are 100 nm, 300 nm and 1000 nm. Hence the relatively small tip-sample separation ($\backsim$ 10 nm) and the thin oxide layer do not significantly deteriorate the measurement signal arising form from the subsurface semiconducting material.

The third method for mapping dopant concentrations that has been used for the present comparison is SSRM. In contrary to the other two techniques the carrier density is measured via resistance changes by the means of a current measurement in contact mode. The main advantage of this approach is its ruggedness with respect to variations in the sample preparation routine due to its self preparing nature. During the measurement, significant forces are exerted by the tip to maintain the current. Hence, the progressive scanning of the same surface area leads to a removal of less conductive surface layers. Thereby the measured spreading resistance after some frames corresponds to a freshly exposed surface and slower depletion and defect accumulation mechanisms do not play a role. On the other hand this strength of SSRM is accompanied by the destruction of the sample, as the surface gets locally etched during the measurement. Compared to the more elegant non-contact techniques that work well under certain experimental conditions but either suffer from preparation induced defects or a less advanced quantification potential, SSRM shows a high reproducibility not only from a qualitative but also from a quantitative perspective. The details of the quantification procedure are following in the next section.

3.1.3 Conclusions

The ability of three different carrier profiling methods that are incorporated in a custom-built AFM system have been assessed in terms of their quantification potential using the example of lightly doped Si Super-Junction test structures. It has been demonstrated that both, non-contact (SCFM, KPFM) and contact mode techniques (SSRM), exhibit an unprecedented sensitivity to map electronically active dopant profiles with concentrations starting form as low as 10^{14} cm^{-3}. Depending on the physical quantity that is measured and in the nature of the employed technique however, differences in the resolution as well as in the quantification capability have been observed. The surface potential measurement as it is applied in KPFM is the most surface sensitive technique and gets therefore more easily distorted by preparation induced defects and surface adsorbates.

KPFM therefore is very good for imaging surface features in conjunction with their impact on the local carrier concentration. On the flip side, however, the quantification of the surface layer often did not correspond to the bulk carrier densities due to their local modification during the preparation of the surface. In this regard, the method is highly dependent on the preparation and ageing of the samples after preparation. In our study, chemical mechanical polishing revealed the best, albeit not perfectly reproducible results for the quantification of dopants by KPFM. In contrast, SCFM measures the capacitance derivative of the combined oxide and depletion layer capacitance system. Hence, the higher information thickness averages out the influence of irregularities at the surface which results in a higher resolution. Nevertheless, this method needs a precise tuning of the external bias voltage since otherwise contrast reversal effects can occur. The best quantitative analyses in this comparison have been achieved by the contact mode SSRM technique. This is attributed to the ruggedness and the self-preparing nature of this method. The local grinding of the native oxide layer by the tip complements to the previous sample preparation processes and therefore enables a high reproducibility of the results. Nevertheless, in future and ongoing work a better understanding of sample preparation induced defects and their passivation mechanisms is targeted, where *e.g.* the application of a surface photo voltage (SPV) [98] showed already very promising results. Furthermore, the capabilities of the here shown methods will be extended to wide band gap semiconducting materials and a plethora of state of the art power devices will be investigated.

3.2 Quantitative dopant imaging, spectroscopy and space charge region observation by SSRM on semiconductor device cross-sections[1]

In previous work [64, 91] it has successfully been demonstrated, that non destructive, non-contact electrostatic force modulation techniques such as Kelvin Probe Force Microscopy (KPFM) [58] or Scanning Capacitance Force Microscopy (SCFM) [62] show a high sensitivity even in the low dopant concentration regime and reveal a clear dopant-induced contrast. The reproducibility of the sample preparation routine and the corresponding surface state density in combination with temporarily occurring capacitive cross-talks [99] however make a reliable quantification of these results difficult. Scanning

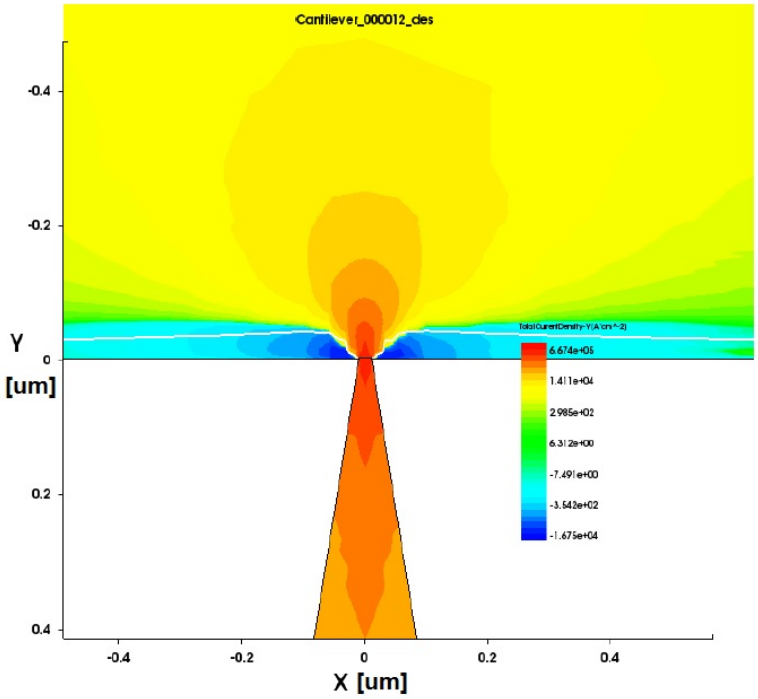

Figure 3.3: A zoom upon the tip-sample contact reveals an electrical focusing effect in the total current density hence resulting in an increased spatial resolution. Figure taken from an unpublished manuscript based on the simulations performed by E. Meyer.

Spreading Resistance Microscopy (SSRM) [65] is less sensitive to deviations arising from hardly controllable preparation parameters due to the abrasive but self-preparing nature of the contact mode operated at high forces, which lead to a phase transformation of a small sample volume right below the tip. The higher conductivity in this region together with the electrical focusing as depicted in (Fig. 3.3) are therefore key to high resolution quantitative carrier profiling. Primarily a quantification procedure [70] based

[1] The results of this section will be submitted to *Applied Physics Letters* (2016).

on calibration curves of well-known staircase structures [69] has been established and recently further extended to small and highly doped devices, such as FinFETs [100], where additional series resistances, that are comparable to the magnitude of the spreading resistance, have to be taken into account [101, 102].
To the best of our knowledge however, there is no previous report about a quantification procedure which considers the influence of a temperature and dopant dependent mobility model. Here, we have applied the Arora mobility model [103] together with simulated temperature values to our experimentaly acquired SSRM data for a precise quantification of the carrier concentration. To demonstrate the strength of this approach we have chosen Super-Junction (SJ) device architectures [94, 104] as they provide an excellent example where ultra-precise dopant profiling is of utmost importance to conclude about the degree of charge compensation in these architectures. The carrier concentration inside the trench can not be determined via monitor wafers, since the epitaxial process is entirely different inside the trench as compared to the planar wafer. Interestingly, the alternating p/n regions of such Super-Junctions are accompanied by depleted space-charge regions (SCR). Since the doping-levels in the p- and n-type regions are determining the spatial extension of the space-charge region around the metallurgic p/n junction, the measured widths can be directly correlated to the dopant concentration in and outside the trench as we elucidate this knowledge here for the first time.

3.2.1 Analysis of the space charge region

For performing SSRM measurements, smoothly across cross-sections of the 'to be investigated' device need to be prepared by a reliable sample preparation routine. The specific chemical mechanical polishing scheme has been defined consequent to the examination of several different preparation approaches for the sample cross-section. This process has also been chosen with respect to a general validity also for more complex crystal structures or materials with hardness close to diamond as it is the case for *e.g.* SiC. To finalize the sample preparation the sample is sputter-etched by Ar ions with an energy of 2 keV on the 'to be probed' surface as well as on the backside of the sample, where the native oxide layer needs to be removed in preparation for the deposition of a low resistive 50 nm thick Al backside contact.
The SSRM measurements as shown in Fig. 3.4c and Fig. 3.4d have been performed under ultra-high vacuum conditions ($p < 10^{-9}$ mbar) in a custom built SPM system [97] with a closed loop scanner that provides a sufficiently large scan range (100 μm x 100 μm laterally and 25 μm vertically) to image the full trench depth of state-of-the-art Super-Junction power device structures. A zoom on the bottom of the trench as depicted in Fig. 3.5a and Fig. 3.5b reveals that our manufacturing approach is able to produce nicely filled trenches without any voids. Furthermore, by comparing horizontal profiles

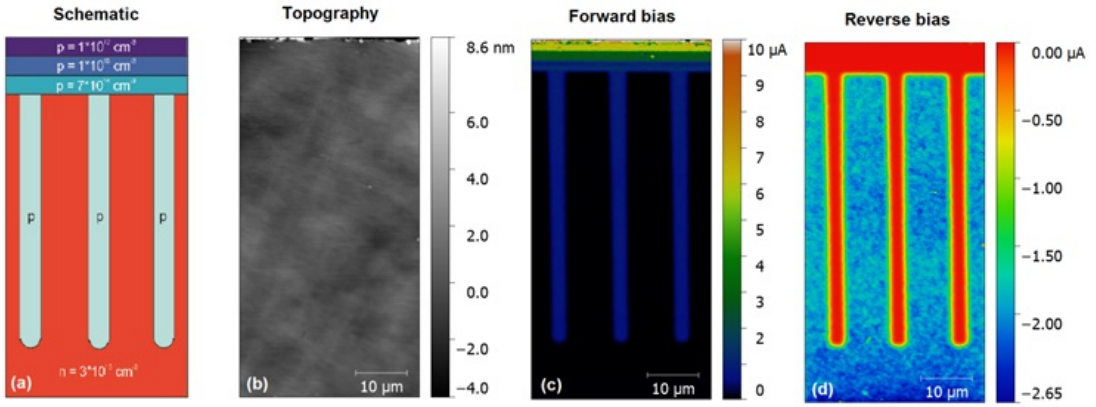

Figure 3.4: (a) A schematic representation of the geometry and the 'as grown' dopant profile of the Super-Junction test samples and the p doped calibration layers embedded in an n type substrate is shown. The simultaneously acquired topographic images (b) display a low surface roughness without showing any characteristic features in the height image of the doped regions. In (c) a positive bias voltage of +3 V is applied to the sample which corresponds to the forward direction of the diode like system. The calibration layers are clearly visible and expectedly disappear if the bias polarity is reversed (d). Figure taken from an unpublished manuscript based on the AFM data taken by U. Gysin.

of such structures one can characterize the width w of the carrier-depleted space charge region (Fig. 3.5c). The depletion width w depends on the dopant concentration of each side of the junction and is given by the expression [105]

$$w = \sqrt{\frac{2\epsilon_s(N_A + N_D)}{qN_AN_D}\left(V_{bi} - \frac{2k_BT}{q}\right)} \tag{3.3}$$

where ϵ_s is the permittivity of the semiconductor, N_A/N_D is the acceptor/donor dopant concentration, q is the elementary charge, V_{bi} is the built-in voltage across the junction, k_B is the Boltzmann constant and T is the temperature. Since the substrate dopant concentration ($N_D = 3 \times 10^{15}$ cm^{-3}) is well-known the application of this formula together with the experimentally determined values for the depletion width allow for a quantification of the carrier concentration inside the trench. The average value for the depletion width, which can be defined as the difference of the full width at half maximum (FWHM) under forward and reverse bias conditions, of three neighbouring trenches is varying between 0.8 μm and 1.04 μm. This width corresponds to a carrier concentration of 7.5×10^{14} cm^{-3} at the trench opening, followed by a linear increase to 1.5×10^{15} cm^{-3} at 20 μm distance from the top. Further down the trench the concentration is again decreasing until reaching 6×10^{14} cm^{-3} at the trench bottom.
Interestingly, as shown in Fig. 3.6a this behaviour is in good agreement with the reverse current characteristics along the trench, while the forward characteristic suggests a decreasing dopant concentration from the trench opening towards the bottom. The mechanism for this behaviour is up to now not well understood and needs further inves-

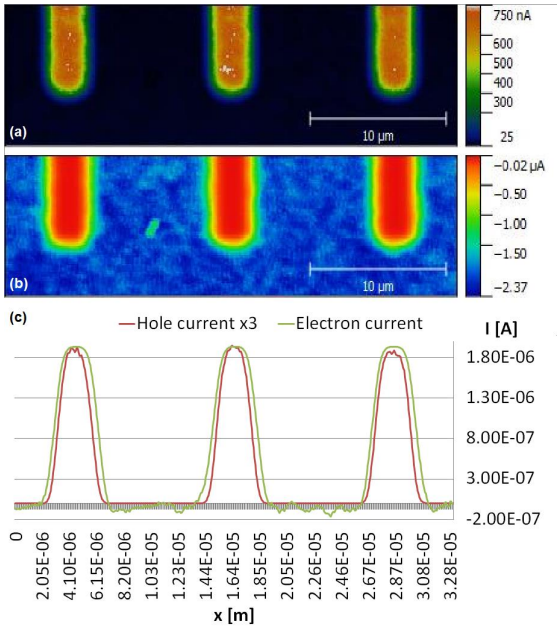

Figure 3.5: The technologically most relevant region at the trench bottom is shown. At a positive bias voltage current is conducted through the p-pillars (a). If the bias polarity gets reversed, the n-type substrate becomes conductive. A comparison of horizontal profiles for these two configurations allows for drawing conclusions on the width of the space charge region, which later on can be related to the carrier concentration inside the trench. The hole current has thereby been multiplied by a factor of three due to the reduced hole mobility. Figures taken from an unpublished manuscript based on the AFM data taken by U. Gysin.

tigation. From a fabrication and preparation perspective it is suggested that the trench opening exhibits a higher dopant concentration since it is rather intuitive that dopants are more easily incorporated there. The polishing with Al_2O_3 particles could also introduce additional acceptor impurities. On the other hand also dopant out-diffusion can take place during the polishing process.

3.2.2 Quantification by means of the Arora mobility model

Beside the analysis of the space charge region that develops at the boundary between p and n-doped pillars a quantification based on the Arora mobility model [103] has been investigated. In contrast to other mobility models the Arora model takes a dopant and temperature dependent mobility into account which needs to be considered in intermediate dopant concentration regimes. For the limiting cases of very high or very low concentrations the mobility is either determined by impurity scattering or phonon scattering. The hole mobility according to the Aroroa model is given by the expression [103]

$$\mu_h = 54.3T_n^{-0.57} + \frac{1.36 \times 10^8 T^{-2.23}}{1 + [N/(2.35 \times 10^{17} T_n^{2.4})]^{0.88 T_n^{-0.146}}} \tag{3.4}$$

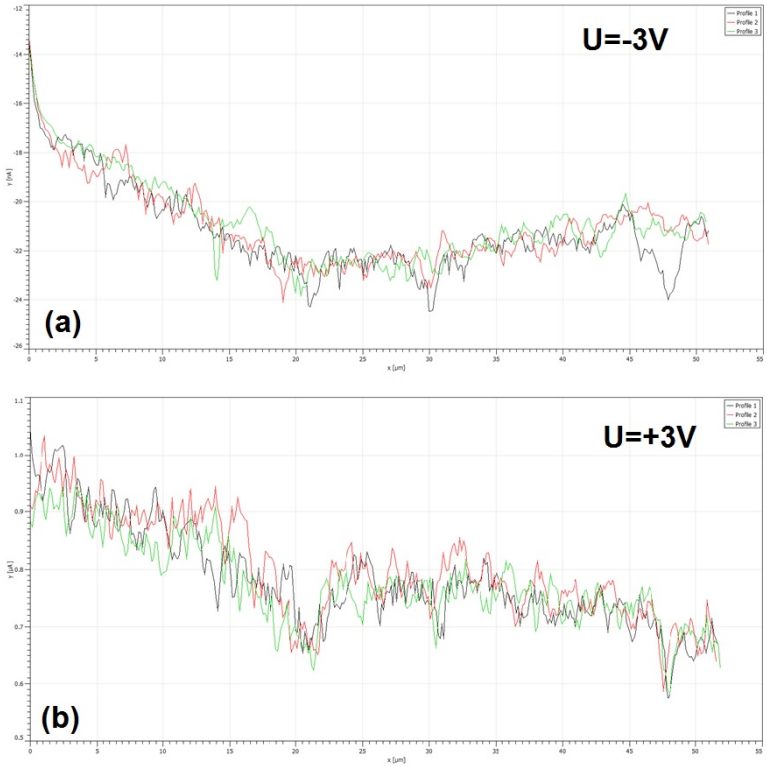

Figure 3.6: The current profiles along the trench for reverse (a) and forward bias (b) conditions are shown. Notably, they behave differently since the current in (a) is negative. Analysis based on the data taken by U. Gysin.

where $T_n = \frac{T}{300}$. The prefactors that are present in this equation have been evaluated by the analysis of experimentally acquired data. By inserting the dopant concentration values for the calibration layers and fitting the $I(p)$ curve (see Eq. 2.11) to the experimental values the electrical radius a can be determined. The current value for each single calibration layer has been fitted according to a histogram of all current values that are present in the SSRM image inside the corresponding layer. This principle is illustrated in Fig. 3.7. In a second step the $I(p)$ curve can be fitted to the experimental values according to Eq. 3.8, however only for one fixed temperature value. It was found that the electrical radius is around 1 nm which is in very good agreement with experimentally determined values for the spatial resolution [106] that can be reached with full diamond tips. Further, simulations of the sample temperature have shown that the temperature increase for p-doped areas is small (around 40 K) and a first approximation at room temperature (RT) is justified. Nevertheless there is one remaining challenge which hinders the read out of the dopant concentration inside the trench. The y_0 offset value which is resulting from the amplifier that is used to measure the output currents is larger than the current values measured inside the trench. To avoid this problem it has been tried to add a fourth point at the origin. The origin in this case means the

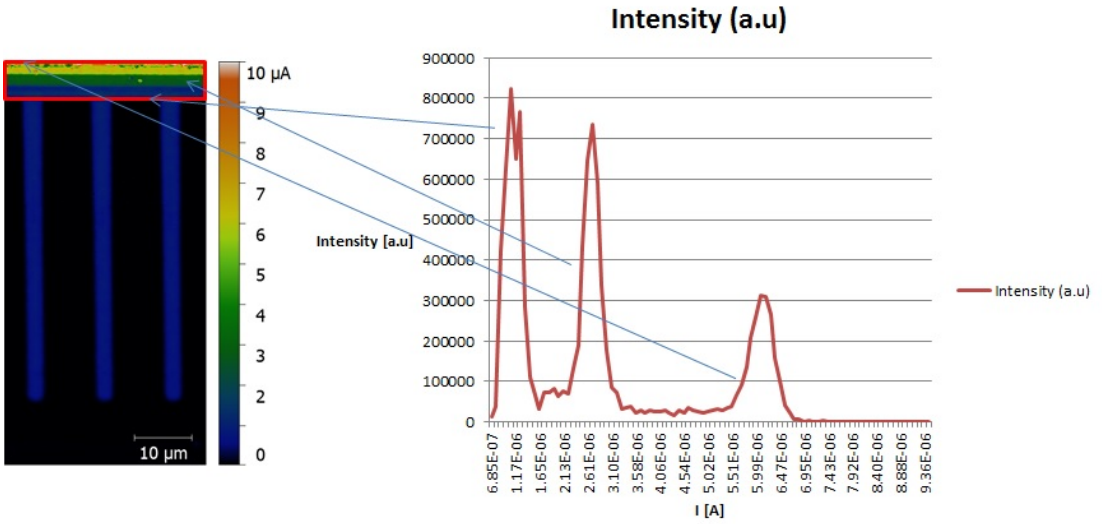

Figure 3.7: The calibration layer current values are determined by a histogram of the present current values in each layer. The fitted peak position was later on used for fitting the electrical radius. Analysis based on the data taken by U. Gysin.

intrinsic carrier concentration of the semiconductor. The deviations from the fit however were significant and it can therefore be concluded that this model is only valid for dopant concentrations that lie in the range between the highest and the lowest dopant concentration of the calibration layers.

3.2.3 Local *I-V* characterization

In a last step the nature of the tip-sample contact has been analysed by recording local *I-V* characteristics in a similar manner as it has been done for the analysis of doped III-V semiconductors [107]. As shown in Fig. 3.9 the various dopant concentrations can clearly be differentiated by means of *I-V* measurements. Further, from the shape of these curves a Schottky behaviour is observed. Therefore these *I-V* characteristics have been analysed regarding the thermoionic emission model [107]

$$I_S = SA^{\star\star}T^2 \exp\left(\frac{-q\Phi_B}{k_B T}\right)\left[\exp\left(\frac{q(V - IR_S)}{nk_B T}\right) - 1\right] \tag{3.5}$$

where S is the contact area, $A^{\star\star}$ is the Richardson constant, Φ_B is the Schottky barrier height, k_B is the Boltzmann constant, T is the temperature, q is the electric charge, V is the applied bias voltage, n is the ideality factor and R_S is the series resistance. The series resistance takes into account the resistance of the undepleted semiconductor as well as of the ohmic contact resistance at the backside. However best fit results have

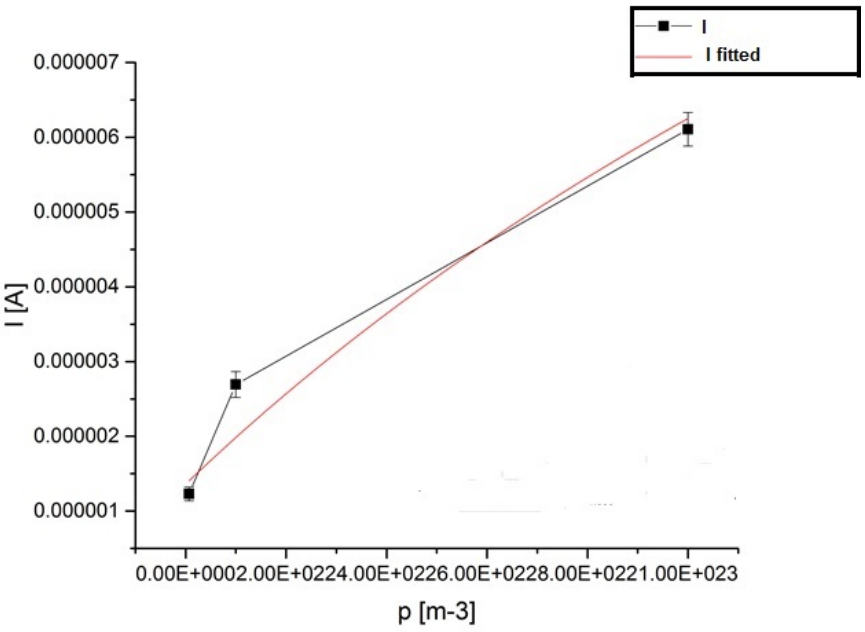

Figure 3.8: The fit for the determination of the electrical radius a from the measured current values of the calibration layers is shown for T=300 °C. Analysis based on the data taken by U. Gysin.

only been achieved by taking a parallel shunt resistance [108] which is of the form

$$I_{sh} = \frac{(V - IR_S)}{R_{sh}} \tag{3.6}$$

into account. According to Ref. [108] this term is considering the presence of a thin oxide layer that is resulting in a carrier accumulation in the semiconductor due to fixed charges in the oxide. By adding this contribution to Eq. 3.6 the experimentally acquired bias sweeps can be fitted more accurately as shown in Fig. 3.10.

The extracted fit parameters are shown in the following table: The extracted resistance

p concentration [cm^{-3}]	n	R_S [Ω]	R_{sh} [Ω]
7×10^{14}	43	2.5×10^{4}	1×10^{10}
1×10^{16}	36	1×10^{4}	9×10^{6}
1×10^{17}	28	3×10^{3}	2×10^{6}

Table 3.1: The fit parameters for each dopant concentration are shown. Notably, the ideality factors n are much higher than for large Schottky contacts. Fitting performed by E. Meyer.

parameters show the right trend since an increased substrate doping will decrease the series resistance. Further suggests the increasing shunt resistance with the dopant concentration that the deviation from a linear behaviour is getting smaller. The large values of the ideality factor however are still not well understood even though it was found that

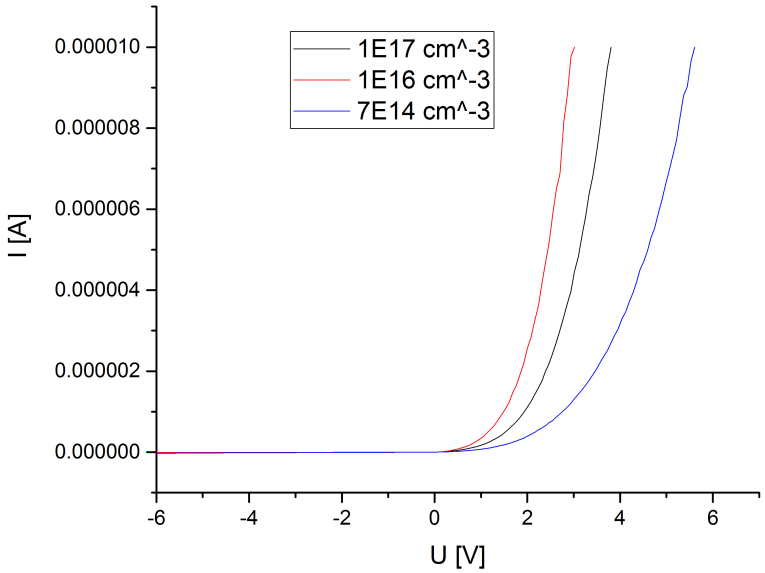

Figure 3.9: The *I-V* characteristics for the differently *p*-doped calibration layers are shown. Data recorded by U. Gysin.

point contact systems exhibit larger values for the ideality factor [109].
As shown in the simulations of Fig. 3.3 there is a hole depleted surface layer present in the proximity of the tip. In experiments on nanoscale *I-V* measurements it has been reported that a surface recombination and generation current can decouple majority and minority currents [110, 111]. While the majority current is flowing across the surface the minority current is flowing along the surface and can be of a similar magnitude or even larger than the actual majority current that is flowing across the interface. In the case reported here the minority electron current is not dominant, however it is likely that the ideality factor is nevertheless influenced.

3.2.4 Conclusions

In this section the quantification possibilities of SSRM measurements have been addressed based on two different methods. On the one hand the alternating pillar structure gives rise to a space charge region at the *pn* junction which can be quantified by the comparison of vertical profiles along the recorded SSRM images under forward and reverse bias. Due to the low dopant concentration inside the trench of the Super-Junction architecture an extended space-charge region could be observed whereof a large fraction is inside the carrier depleted trench.
On the other hand a quantification procedure based on the Arora mobility model has been introduced. By the use of three layers of well-known dopant concentration the

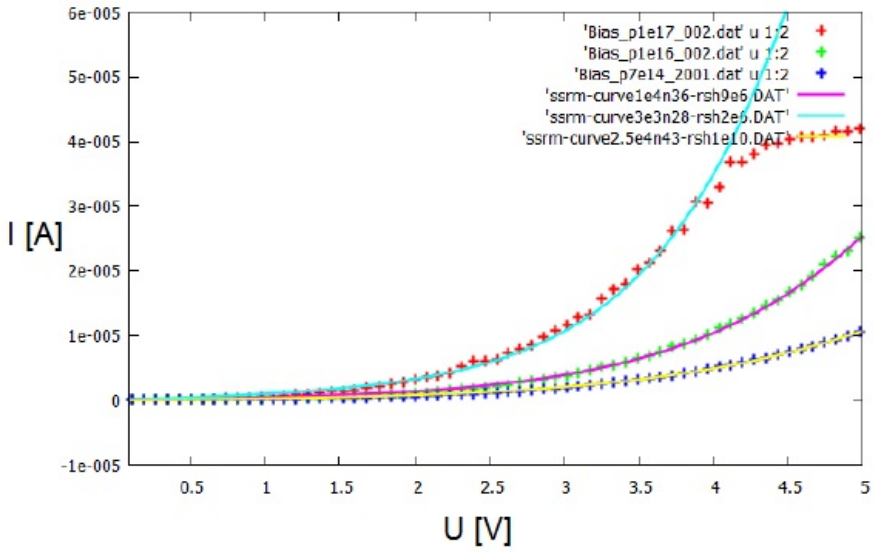

Figure 3.10: The experimentally acquired *I-V* data is shown up to a bias voltage of 5 V and compared to the corresponding fit that is taking a series and parallel resistance into account. Analysis performed by E. Meyer.

measured current could be fitted as a function of the dopant concentration. The impact of Joule heating has been simulated and was found to be small, which justified a first approximation at RT. The electrical radius a and the y_0 offset due to the used amplifier for the current measurement were thereby the only fit parameters and the electrical radius was in good agreement with the literature.

At this point however it is hard to judge which method shall be preferred in terms of the quantification of dopant profiles inside the trench since further challenges need to be overcome. While for the first method the correlation of the width of the SCR along the trench and the corresponding current profiles needs further investigation the second method was currently suffering from an inappropriate choice of the dopant concentrations of the calibration layers. Also attention has to be paid on the nature of the tip-sample contact which is showing rather a Schottky than an ohmic behaviour. For this nanoscale Schottky contacts so far the best agreement between the experimental and theoretical values has been achieved by considering a parallel shunt resistance that take the presence of a thin oxide layer with fixed positive charges into account. The high ideality factors might be caused by minority electron currents that spread along the surface and influence the *I-V* characteristics across the contact itself.

CHAPTER 4

Characterization of active device areas in 4H-SiC

Within this chapter electronically active dopant profiles of epitaxially grown n-type 4H-SiC calibration layer structures with dopant concentrations ranging from 3×10^{15} cm^{-3} to 1×10^{19} cm^{-3} have been investigated by non-contact Scanning Probe Microscopy (SPM) methods. It has been shown that Kelvin Probe Force Microscopy (KPFM) and Electrostatic Force Microscopy (EFM) are capable of resolving two-dimensional carrier maps in the low doping concentration regime with high spatial resolution. Furthermore, different information depths of this wide band gap semiconductor material could be assessed due to the inherent properties of each profiling method. Additionally a resolution enhancement has been observed under laser illumination which was attributed to reduced band-bending conditions. To gauge the SPM signals, epitaxially grown layers were primarily calibrated in terms of their dopant concentration by C-V measurements. Further, the shielding cell-architecture of a buried grid (BG) Junction Barrier Schottky (JBS) diode consisting of multiple consecutive p^+-implanted stripes below the interface of the metal/semiconductor junction has been investigated by performing non-contact Scanning Probe Microscopy (SPM) and Secondary Electron Potential Contrast (SEPC) measurements on device cross-sections. It has been shown that these techniques are capable of mapping two-dimensional (2D) carrier distributions inside the active device area, however with different resolution and quantification possibilities.

4.1 Two-dimensional carrier profiling on lightly doped n-type 4H-SiC epitaxially grown layers[1]

The functionality and the electronic performance of basically any semiconductor device strongly depend on the dopant profile, in particular on the spatial distribution of the electronically activated fraction of impurity atoms incorporated into the lattice of the host crystal. In power semiconductors, the two main figures of merit are (i) a high blocking capability, which minimizes the reverse-current in the OFF-state and (ii) a low ON-state resistance when the device is operated under high current density. This performance requirement can be either met by highly demanding trench etch and refill processes [94] in charge-compensated silicon Super-Junction power devices [93] or by a change to wide band gap materials with their superior material properties [33] in device manufacturing.
Power semiconductor punch through diodes, designed to shape the E-field under reverse-bias conditions in form of a trapezoid, typically consist of three differently doped n-type layers to fulfil maximum performance requirements in terms of the highest breakdown voltage. Especially the lightly doped drift layer, which on the one hand absorbs the major contribution of the breakdown voltage while on the other hand limits the forward conduction through its high resistivity, plays a crucial role for the device performance.
In this contribution, we therefore primarily assess carrier profiles of n-type 4H-SiC calibration layer structures in this low dopant concentration regime either by the extraction of the slope from Capacitance-Voltage (C-V) measurements or by means of non-contact SPM techniques [112] which have demonstrated their ability to image carrier profiles in two dimensions over the full dynamic range with high spatial resolution.

4.1.1 Epitaxial growth

Epitaxial growth of n-type calibration layers was performed on commercially available 4H-SiC substrate wafers in a chemical vapour deposition (CVD) reactor with wafer rotation. The layers were grown at temperatures of 1600 °C with silane and propane as precursors and hydrogen as the carrier gas. Nitrogen gas was used to achieve the targeted donor concentration in the conducting layers. The resulting calibration-layers (see Fig. 4.1) consisted of a stack of 2 μm thick, nitrogen doped layers starting with a 1×10^{18} cm^{-3} doped buffer layer, then a 3×10^{15} cm^{-3} lightly doped layer, a 1×10^{16} cm^{-3} doped layer, and finally a 1×10^{18} cm^{-3} doped top layer. The substrate doping is typically in the range of 1×10^{18} cm^{-3} to 1×10^{19} cm^{-3}.

[1] The results of this section were published in *Materials Science Forum* **821-823**, 269 (2015).

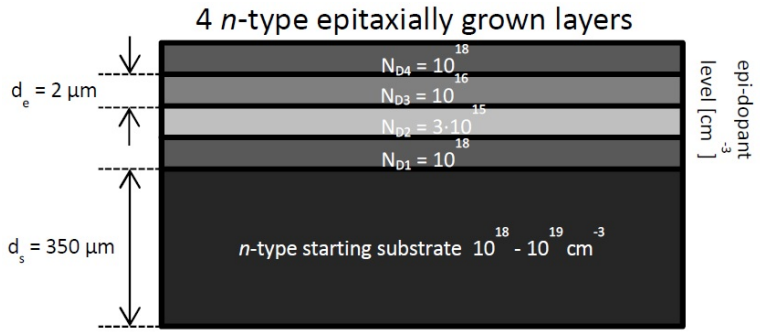

Figure 4.1: Schematic view on the differently doped n-type calibration layers on top of a 350 μm thick n-type substrate. Figure taken from [91].

4.1.2 *C-V* characterization

The adjustment of the nitrogen dopant flow for the different calibration layers was performed by separately growing epitaxial layers with doping concentrations of different orders of magnitude. Subsequently, the fabrication of nickel Schottky contacts (d = 500 μm) evenly distributed across the wafer was prepared by a photolithographic lift-off deposition process. C-V measurements were performed on more than 300 of these Schottky contacts per grown wafer to analyse the net doping concentration (electrically active nitrogen donor concentration minus the concentration of compensating acceptors) of the first three calibration layers. Fig. 4.2 shows the doping-depth profile determined from the slope of the measured C-V curves. The depth-profile reveals two layers having a net doping concentration of 1×10^{16} cm^{-3} and 3×10^{15} cm^{-3}, and a thickness of 0.6 μm and 1.0 μm, respectively. From Fig. 4.2 it can be seen that the net doping concentration varies across the wafer. A wafer map of the doping uniformity can be created (Fig. 4.2b)

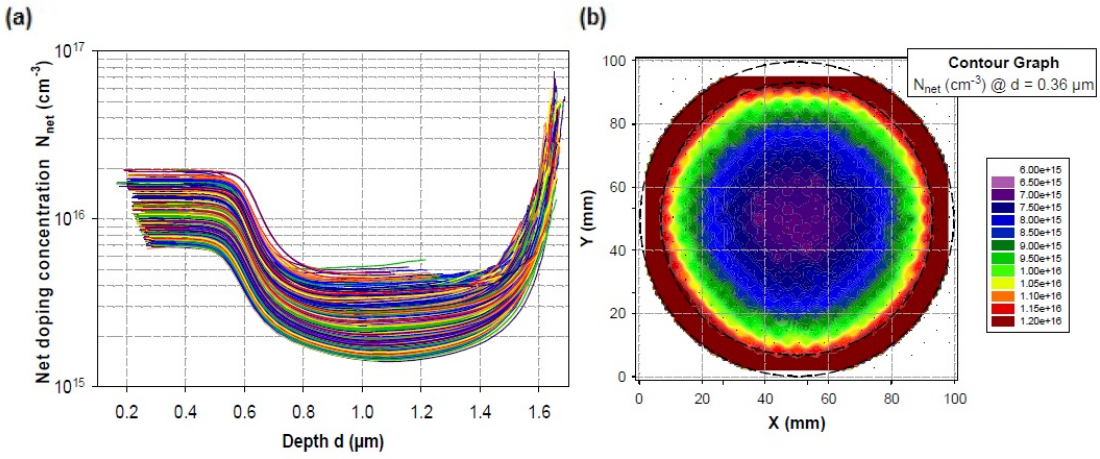

Figure 4.2: (a) Net doping depth-profile derived from C-V measurements on more than 300 Schottky contacts evenly distributed over the first 3 epitaxial layers grown on a 100 mm diameter 4H-SiC wafer. (b) Wafer map of the net doping concentration in a depth of 0.36 μm from the surface. The wafer map is derived from the depth profiles shown in (a). Figure taken from [91].

by extracting the net doping concentration at a certain depth of the profile and plot it as a function of the Schottky contact position. Due to the rotation of the wafer during the growth process, the doping uniformity exhibits a rotational symmetry. In our case, the center circular area with 80 mm diameter (10 mm edge exclusion) has an average net doping concentration of 8.47×10^{15} cm^{-3} at a depth of 0.36 μm and a standard deviation over mean uniformity of 12% (Dopant range: $7.14 \times 10^{15} - 10.51 \times 10^{15}$ cm^{-3}).

4.1.3 SPM-Based two-dimensional carrier profiling

The working principle of KPFM [58] and EFM [90] is based on their sensitivity to different electrostatic force components with differing characteristic information depths which arise under the influence of an external bias voltage $V = V_{DC} + V_{AC} \times \sin(\omega t)$ between the tip and the sample:

$$F_\omega = -\frac{\partial C}{\partial z}(V_{DC} - V_{CPD})V_{AC}\sin(\omega t) \tag{4.1}$$

$$F_{2\omega} = \frac{\partial C}{\partial z}\frac{V_{AC}^2}{4}\cos(2\omega t) \tag{4.2}$$

Due to the variety of different possible cleaving planes in 4H-SiC, cross-sections were prepared by a grinding step followed by chemical mechanical polishing with diamond particles in different grain sizes and a Syton SF1 finish, which resulted in a sub-nanometer surface roughness (Fig. 4.3a).

Nevertheless, as shown in Fig. 4.3b, fine scratches due to our preparation method still remain visible in the compensating DC bias image influencing the measured values for the Contact Potential Difference (CPD), while in the amplitude signal of the EFM image (Fig. 4.3c) this effect gets less pronounced. This can be attributed to the influence of the capacitance variation on the different force components. Since for KPFM measurements the CPD gets compensated by an external DC bias, the F_ω force component (Eq. 4.1) vanishes and with it the influence of changes in the capacitance signal. In contrast, the response of the semiconductor material to the oscillating term by the external bias voltage induces periodic accumulation and depletion of free charge carriers resulting in a variable depletion layer capacitance. Hence, the amplitude of the $F_{2\omega}$ component (Eq. 4.2) is probing rather extended depletion layers, whereas KPFM is very sensitive to surface defects and adsorbates.

Our measurements were performed under ultra-high vacuum (UHV) conditions, which enabled us to simultaneously acquire topographic images (Fig. 4.3a), due to the high Q-factor of the first and second resonance frequency of the PtIr-coated Nanosensors PPP-NCLPt cantilever optimized for dynamic mode operation. Further details on the experimental setup are published elsewhere [97]. Since there are no topographic features visible, we attribute the nature of the physical contrast (Fig. 4.3b,c) to a pure dopant

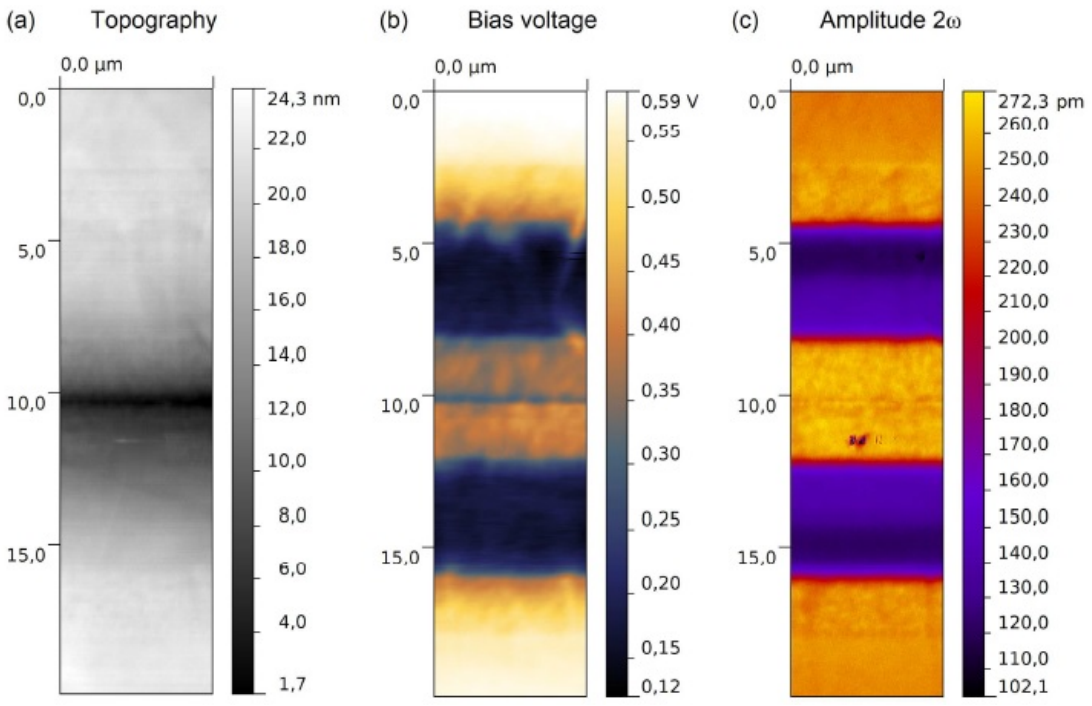

Figure 4.3: Simultaneously acquired topographic image (a) while KPFM (b) and 2ω EFM (c) measurements were performed by the oscillation of the second eigenmode. To avoid rounding effects at the sample edges two samples were glued together with non-conductive epoxy. Figure taken from [91].

effect. In KPFM, the measured $CPD = (\Phi_s - \Phi_t)/q$ allows for drawing conclusions about the dopant dependent work function of the inspected sample, while in EFM, the charge carrier concentration of the sample affects the magnitude of the amplitude signal. Differences between the second ($N_{D2} = 3 \times 10^{15}$ cm $^{-3}$) and the third ($N_{D3} = 1 \times 10^{16}$ cm $^{-3}$) epitaxially grown calibration layer corresponding to a calculated $\Delta CPD \approx 31$ mV could be resolved.

Still, the transition region in the KPFM image (Fig. 4.3b) gets smeared out due to surface defects, which makes it difficult to determine the position of the metallurgical junction. This effect can be illustrated in the energy band diagram (Fig. 4.4a) of the tip-semiconductor system. Defect states within the band gap influence the position of the Fermi level resulting in an increased sample work function. However, almost ideal flatband conditions (Fig. 4.4b) can be restored by illuminating the sample with laser light ($\lambda = 500$ nm with 50 nm bandwidth, 2.5 W/cm^2 intensity). The diffusion of photo-generated electron-hole pairs towards the surface creates a Surface Photo Voltage (SPV) [98], which counteracts the defect-induced work function increase. As can be seen in the KPFM image of the same structure under illumination (Fig. 4.4c) a significant contrast enhancement especially at the border between two differently doped layers was achieved due to the interaction with laser light.

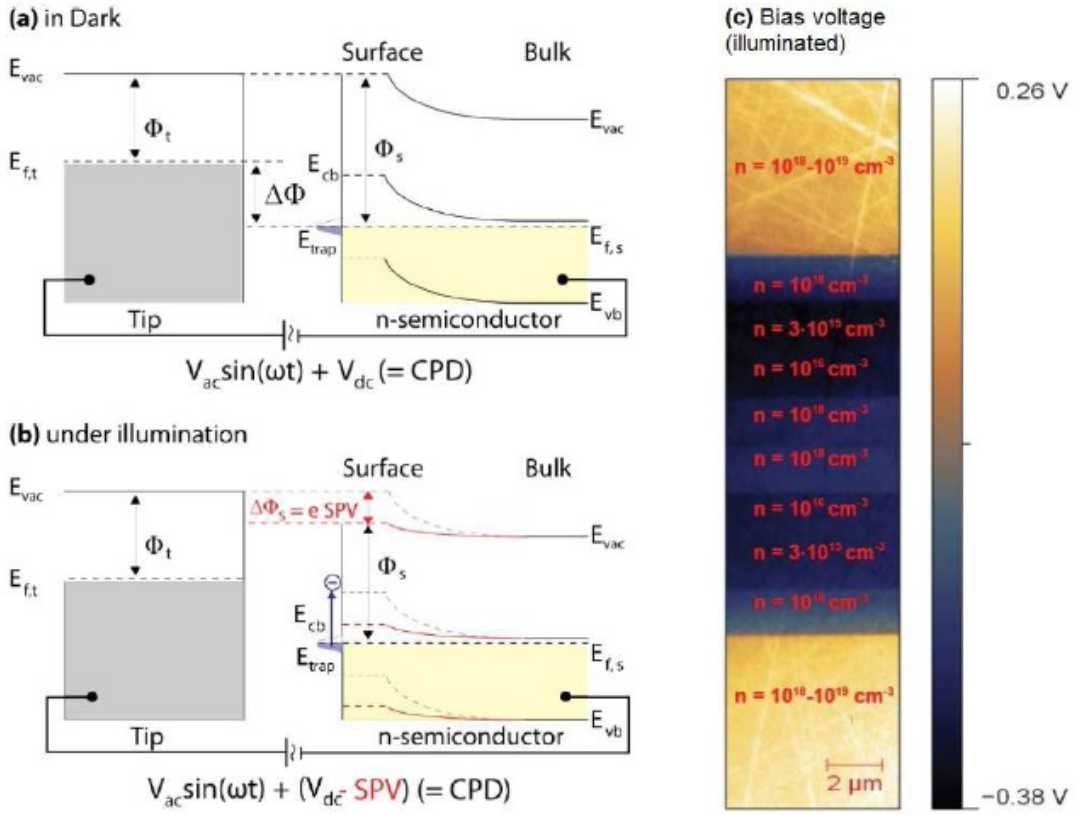

Figure 4.4: Energy band diagrams without (a) and with (b) laser illumination taken from [113]. KPFM image (c) under reduced band bending conditions. Entire figure taken from [91].

4.1.4 Conclusions

It is important to note that the influence of dopant depletion or accumulation together with other surface defects needs to be controlled. Their influence here is, as demonstrated, low enough to avoid complete pinning of the Fermi level, but nevertheless compromises the quantification of bulk dopant concentrations as measured by C-V measurements with low lateral resolution. In this contribution we have shown that SPM methods such as KPFM and EFM are highly valuable complementary tools to investigate low n-type dopant concentrations of 4H-SiC calibration layers with high spatial resolution. The probed physical quantity of these methods is different *i.e.* they involve Schottky transport, work function and capacitance measurements with different lateral resolution but also differ in their information depth. The latter is thereby restricted to single atomic layers in C-V measurements and KPFM and slightly less critical for EFM measurements. While for C-V measurements the large contact area and the nature of the dopant concentration extraction from the slope $1/C^2(V)$ minimize the contribution of surface states, in KPFM a distortion of the measurement results due to defect-induced band bending could be overcome by the application of a SPV resulting in a passivation

of surface states and therefore in a significant enhancement of the resolution.

4.2 Junction Barrier Schottky (JBS) Rectifier Interface Engineering Facilitated by Two-Dimensional (2D) Dopant Imaging[2]

State-of-the-art energy efficient power conversion systems for traction or medium voltage drive applications (e.g. 3.3 kV application voltage) require an energy efficient rectifier solution. Such a technology should offer low switching losses during the reverse recovery as well as superior static characteristics such as a low ON-state voltage drop and a low leakage current level in the OFF-state. While SiC Schottky Barrier Diodes (SBD) are able to outperform Si p-i-n diodes in terms of switching speed due to their unipolar nature and specific ON-resistance for high breakdown voltages due to the beneficial material properties of SiC, these devices suffer from relatively large leakage currents for reverse-voltages above 1.5 kV [114]. Mainly the almost an order of magnitude higher (as compared to Si) electrical field E at the interface between the carrier-depleted wide band gap material and the Schottky-metal has an undesired impact on the shape of the Schottky barrier $\Phi_{B,n}$ which connects the quantum mechanical energy levels of the semiconductor and the metal. Image force induced barrier lowering [61] facilitates thermionic emission for low electric fields while Fowler-Nordheim tunneling [61, 115] is the dominant leakage mechanism at high reverse voltages close to avalanche breakdown.

4.2.1 JBS device design

The Junction Barrier Schottky (JBS) [116] architecture (Fig. 4.5) diminishes the influence of the image force by employing highly doped p^+-areas to effectively shield the Schottky-interface from high E-fields. The working principle of this p^+-implanted grid pattern inside the drift layer can be understood as a superposition of reverse biased pn junctions whose depletion fronts merge to sustain high cathode voltages along the whole device. In forward direction this design has two different effects. On the one hand due to the suppression of Schottky-barrier lowering a metal characterized by a lower Schottky-barrier height in contact to the 4H-SiC crystal can be chosen to reduce the ON-state voltage drop, while on the other hand an electron current can only flow between the p^+-regions which leads to an increase of the specific ON-resistance.

Therefore, the trade-off between the active area consumption of these p^+-grids and their shielding effect has been precisely analysed and optimized by means of numerical simulations [118]. It was found that the Schottky-contact can be most effectively shielded by narrow and deeply implanted p^+-areas. In this contribution, we investigate a recent descendant of this device architecture, namely the buried grid (BG) JBS design [119].

[2]The results of this section were published in *Materials Science Forum* **858**, 497 (2016).

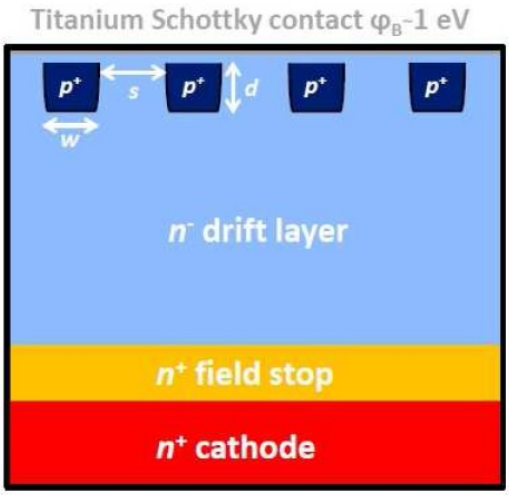

Figure 4.5: Schematic view of the sample cross-section of a BG-JBS diode structure. The width w, the spacing s and the depth d of the p^+-implanted regions inside the active area determine the device performance. Figure taken from [117].

By shifting the p^+-grid from the surface deeper into the drift layer, a further reduction of both, the electric field E underneath the Schottky-contact and the specific ON-resistance, can be accomplished which is beneficial for the overall device performance. To avoid floating p^+-areas that are sacrificing the surge-current moderation [118, 120] offered by a biased minority carrier injection, the BG is interconnected trough feeders to the top electrode. However, due to dopant diffusion and activation, the information on the electronically active dopant profile used as input parameter for numerical simulations might change entirely. It is therefore inevitable to map the 2D dopant profile to draw conclusions about the final electronic device performance.

4.2.2 Fabrication

The p^+-grid inside the active area of the device was manufactured by cascaded ion implantation of a 1 μm deep box profile (red rectangle in Fig. 4.6) with an Al concentration in the range of 5×10^{19} cm^{-3} through a 2 μm thick lithographically patterned SiO_2 hard mask layer. The implantation step was carried out at elevated temperatures of 500 °C to prevent crystal amorphization and with the direction of the incident ion-beam perpendicular to the wafer surface. Due to the substrate mis-cut angle of 4 ° with respect to the crystallographic c-axis, the latter ensures an effective implantation angle which abandons undesired channelling effects. The subsequent activation annealing and epitaxial re-growth can be combined into one processing step, since the parameters are similar (1600-1650 °C, 10-15 min). The top 2 μm thick n-type layer has been epitaxially re-grown by using silane-propane chemistry, incorporating nitrogen dopant atoms.

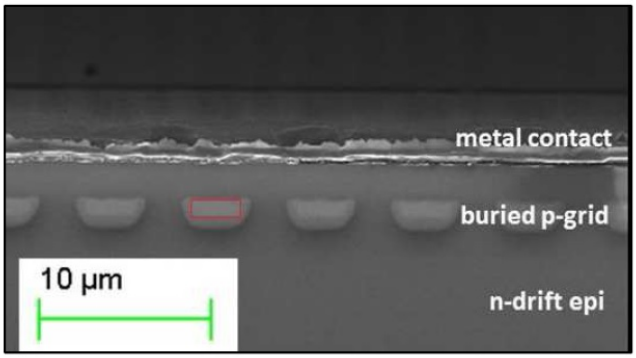

Figure 4.6: Electrograph of the sample cross-section of a BG-JBS diode structure. The width w, the spacing s and the depth d of the p^+-implanted regions inside the active area determine the final device performance. Figure taken from [117].

4.2.3 Two-dimensional dopant imaging

In this contribution we utilize complementary dopant observation techniques based either on a commercial Secondary Electron Microscope (SEM) and its ability to map the potential contrast between oppositely doped regions or on a custom-built Scanning Probe Microscope (SPM) [97] which is an even more versatile tool to directly observe dopant concentrations by different physical contrast mechanisms even in the low dopant concentration regime [121].
Cross-sections of cleaved BG-JBS structures in 4H-SiC were investigated after a solvent based cleaning process followed by an UV-ozone treatment. Fig. 4.6 shows the dopant contrast between the p^+-grid inside the n-type drift region, which is a consequence of the band bending in the junction-SEM-system resulting in a different energy spacing with respect to the detector [122]. Impressively, the electrograph clearly resolves the 1 μm deep peak doping concentration as visualized by the bright contrast inside the p^+ JBS cells (Fig. 4.6). According to Eq. 4.3,

$$E_p = E_n - qV_{bi} \tag{4.3}$$

where $E_{p,n}$ is the energy required for valence band electrons from p and respectively n doped areas to reach the detector level, q is the elementary charge and V_{bi} is the built in voltage, secondary electrons emitted from the p^+-areas require by the amount of qV_{bi} less energy to reach the detector. Therefore the technique provides better contrast in wide band gap (WBG) semiconductors. Due to the larger secondary electron current these areas appear brighter than the surrounding drift-layer. For an optimized contrast, however, energy filtering to cut-off the high energy tail of the signal has to be applied, which limits the quantification possibilities of this method [122].
On the contrary, raw data collected by non-contact SPM techniques such as Kelvin Probe

Force Microscopy (KPFM) [58] and Scanning Capacitance Force Microscopy (SCFM) [62] can be directly utilized to map changes in the oscillatory electrostatic force (ESF) signal with high precision and are therefore offering quantification opportunities. As compared to contact mode, these SPM methods are able to bypass the problem of forming a stable electronic contact due to the immense hardness of SiC. However, also contact mode techniques have been successfully applied to map dopant densities [123]. By means of a lock-in technique separate components of the ESF,

$$F_{esf} = -\frac{\partial C}{\partial z}\left[\frac{1}{2}(V_{DC}-V_{CPD})^2+\frac{V_{AC}^2}{4}\right]-\frac{\partial C}{\partial z}(V_{DC}-V_{CPD})V_{AC}\sin(\omega t)+\frac{\partial C}{\partial z}\frac{V_{AC}^2}{4}\cos(2\omega t) \tag{4.4}$$

where C is the tip-sample capacitance, $V_{DC,AC}$ is the direct and respectively alternating current term of an external bias voltage, $V_{CPD} = (\Phi_{sample} - \Phi_{tip})/q$ is the contact potential difference (CPD) and ω is the angular frequency, can be adressed to characterize the electronic properties of the sample.

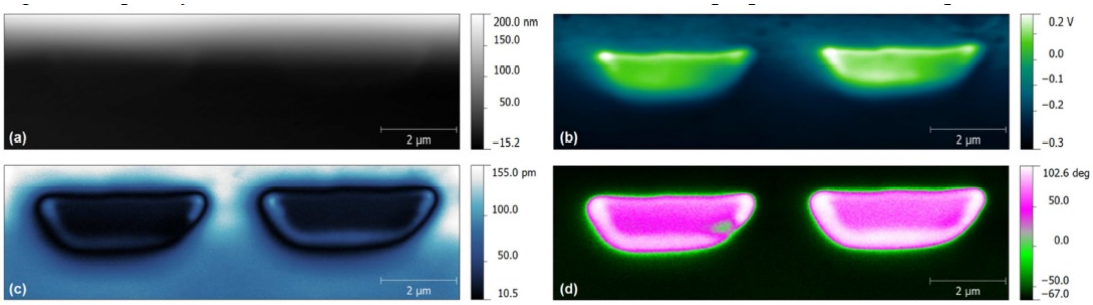

Figure 4.7: Comparison of the topography (a), KPFM (b) and SCFM (c,d) images of our sample cross-section. While both methods clearly show the dopant contrast of two adjacent p^+-areas, the KPFM image (b) shows a smaller cross section as compared to the amplitude (c) and phase images (d) of SCFM. This can be attributed to the high surface sensitivity of KPFM in contrast to the ∼nm information depth of SCFM. Figure taken from [117].

For KPFM, on the one hand, the read out of the dopant dependent CPD can be easily performed by recording the V_{DC} values that are needed to nullify the second term of Eq. 4.4. The contrast, as shown in Fig. 4.7, is mainly attributed to a dopant effect since in the topographic image (Fig. 4.7a) no well-like structures were observed. However, the junctions in the CPD image (Fig. 4.7b) are blurred out due to surface defects and adsorbates causing strong band bending. Although the difference between p-type and n-type regions could be nicely observed and V_{CPD} was found to be ∼0.38 V, the quantification of these results remains difficult due to the aforementioned undesired surface effects.

On the other hand, SCFM (Fig. 4.7c,d) is mapping the capacitance variation of the last term of Eq. 4.4 with respect to an external stimulus. Therefore, the capacitance derivative is expanded into a z and a V dependent contribution [12] and the response of the latter to an AC voltage is investigated. With this method the influence of the doping

concentration upon the variable depletion layer capacitance can be studied especially in the low doped regime, since those regions show a higher amplitude signal due to the greater change in the capacitance derivative signal. Hence, the highly doped p^+-regions in Fig. 4.7c appear darker than the lightly doped drift layer. Interestingly, additional features at the border of our structures have been observed. The contrast of these features gets even more pronounced in the SCFM phase image which contains information about the dopant characteristics (n or p). According to previous studies [124], we attribute this effect to a bias dependent contrast reversal which is more likely to occur in WBG materials such as 4H-SiC due to their higher interfacial trap density. Similar to KPFM, SCFM is offering a quantification potential as this technique inherently involves local capacitance spectroscopy measurements. However, further theoretical studies are necessary and until now a quantification is only possible by a comparison to precisely gauged calibration samples that were beforehand analyzed by C-V measurements [91].

4.2.4 Conclusions

Dopant concentration profiles are designed and manufactured to determine the electronic behavior of every semiconductor device. Notably it is difficult to warrant their 3D distribution within the device during manufacturing and during cyclic use. Here, SPM-derived methods allow for a unique access to dopant profiles along cross-sections of basically every device architecture. The present results on BG-JBS devices in SiC evidence that topographic, capacitive and surface potential contributions regarding the dopant density can be separated and analyzed. The observed differences in the resolution can be attributed to the underlying physical mechanism that is utilized for the observation. While KPFM is a surface sensitive technique that critically depends on the sample preparation, SCFM is probing rather extended depletion layers, therefore averaging out surface-distortions induced by the sample preparation and making it a quite attractive candidate for quantitative dopant mapping. In comparison to SEPC images the two SPM signals exhibit much more quantitative results. However, for routine measurements to observe the profile shape, SEPC provides a quick alternative as compared to SPM-based methods.

In ongoing and future studies, the contrast mechanisms, the resolution and the feasibility of calibrated dopant maps shall be explored. Additionally, different device segments of device architectures at different stages of manufacturing and use provide very interesting specimens to reveal further insights into the atomistic processes in conjunction with dopant implantation and diffusion. Thus, these techniques open up new possibilities to investigate semiconductor and device physics down to the level of ultra-low dopant concentrations and with nanometer scale resolution.

CHAPTER 5

On the assessment of channel mobilities in 4H-SiC trench MOSFETs

The aim of this chapter is to combine the U-MOSFET design with its U-shape trench-gate architecture which is well established in silicon technology and benefits from a reduction in cell pitch size as well as from the elimination of the junction-FET region with the superior material properties of 4H-SiC. While current planar SiC MOSFET devices are challenged by a high ON-state resistance caused by relatively poor channel mobilities due to different scattering processes at the 4H-SiC/insulator interface, our hybrid approach benefits by the normal carrier injection in the inversion channel formed along the $\{11\bar{2}0\}$ direction which exhibits a higher channel mobility. In the following paragraphs focus will be given on special lateral test structures which have a similar architecture as compared to vertical power devices but enable an exclusive characterization of the channel mobility. In vertical power devices however only the total ON-resistance which consists of various different resistance components can be assessed. Numerical simulations on the trench width and the gate insulator thickness have been performed to study their influence on the electronic performance. Furthermore, a brief insight on the dry-etching process of trench structures in 4H-SiC will be given.

5.1 Device simulations on novel high channel mobility 4H-SiC trench MOSFETs and their fabrication processes[1]

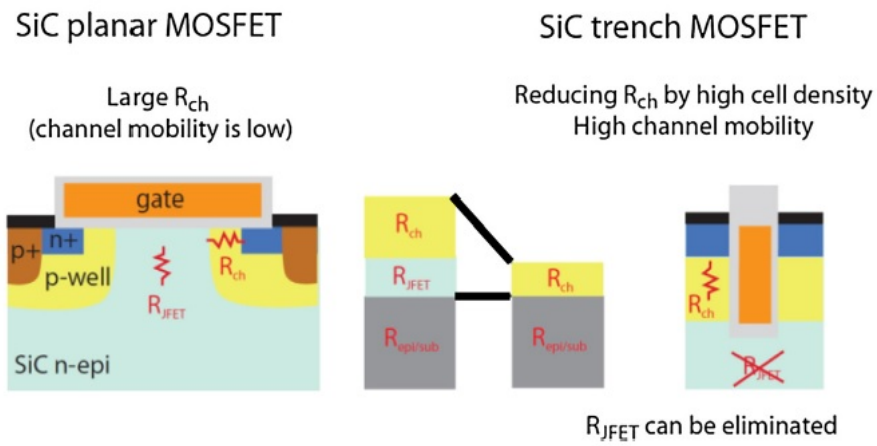

Figure 5.1: Schematic view of the planar and trench MOSFET device cross-sections with the corresponding resistance components for each of the microscopic device cell-architectures. Figure taken from [125].

High charge carrier mobilities inside the inversion layer of MOS-controlled semiconductor devices are able to beneficially influence the ON-state resistance when the device is operated under forward bias conditions, which is beside a high blocking voltage capability above 1 kV one of the two main figures of merit of power semiconductor devices. In silicon technology, state-of-the-art charge-compensated Super-Junction devices, improved the trade-off between these two entities [49] beyond the so-called unipolar silicon limit [48] at the cost of highly demanding manufacturing processes. For power applications the higher cost is either incurred from a sequence of epitaxial layer deposition and implantation steps completed by dopant diffusion [126–128] to form continuous pillars or from trench etching and epitaxial-refilling processes [129], where recently trenches as deep as 60 μm have been demonstrated [94]. Nevertheless, the performance of these devices remains limited by the intrinsic material properties of Si. Alternatively, wide band gap materials such as SiC with their superior material properties [33] are much more suitable for power semiconductor applications. Mainly, the almost an order of magnitude higher critical electric field and the high thermal conductivity motivated the development of SiC based unipolar power devices (*e.g.* planar MOSFETs and Schottky diodes). Their fundamental building block is the 4H-SiC crystal polytype which exhibits the highest bulk mobility and offers the most mature epitaxial growth and processing technology beside the aforementioned advantages. SiC MOSFET devices have demonstrated their potential in terms of low power dissipation [130] and are now commercially

[1]The results of this section were published in *Microelectronic Engineering* **145**, 166 (2015).

available. Even for the 650 V voltage-class they challenge the established Si Super-Junction architecture [131].
However, the performance of current SiC MOSFET devices is challenged by relatively poor channel mobilities [43] which are significantly reduced compared to the bulk value of 950 cm^2/Vs, due to interface trap states (D_{it}) [132] causing scattering processes at the 4H-SiC/insulator interface [133]. Furthermore, the parasitic junction-FET resistance R_{JFET} (as shown in Fig. 5.1) which arises by the constriction of charge-carriers in close proximity to the well regions causes an increasing ON-state voltage drop for increasing MOS-injector cell-density when the device is operated in forward direction. In contrast, the channel, accumulation and drift-region resistances of the U-MOSFET with a U-shape designed trench-gate architecture, well established in silicon technology, benefits from a reduction of the cell pitch and from the completely eliminated junction-FET resistance [34]. Moreover, this design enhances the device performance by the normal carrier injection in the inversion channel formed along the $\{11\bar{2}0\}$ direction which exhibits a higher channel mobility as compared to the perpendicular c-axis [134] which is commonly utilized for planar devices. Hence, the combination of these favourable aspects facilitated the development of the next generation of trenched power semiconductor devices [135].
In this contribution we focus on special lateral test structures which have a similar architecture as compared to vertical power devices but enable us to exclusively characterize the channel mobility in the inversion layer. In vertical power devices, in contrast, only the total ON-resistance which consists of various different resistance components can be assessed. We present optimized simulations of 4H-SiC trench MOSFET structures, with 3 μm trench depth and trench widths ranging from 500 nm up to 3 μm. Our models set up the design parameters for the manufacturing process such that the electronic performance of the fabricated devices can be benchmarked against the numerical counterparts. Additionally, the influence of the gate insulator thickness as well as of the interface trap density on the device performance (*e.g.* threshold voltage) will be discussed. Finally, a brief analysis will be given on the dry-etching process focusing on the plasma structuring of trench structures in 4H-SiC.

5.1.1 Device performance simulations

We compare the channel mobilities of our trench-designs against the channel mobility of a planar design as established in state-of-the-art SiC MOS-based power-devices (Fig. 5.1). This numerical comparison has to be performed under the constraint of avoiding localized peaks of the electric field distribution during the reverse bias operation of the device since the source-areas are exposed to a very high E-field. Field-crowding would lead to a breakdown of the device already at low voltages applied in the blocking direction. Localized peaks in the E-field can be circumvented either by the introduction of rounded

trench corners at the bottom of the trench which we utilized for our simulations or by special bottom oxide protection [136] or a thick bottom oxide [137]. Additional boundary conditions on the trench geometry were set by our lithographic and manufacturing tools. For our numerical simulations we therefore varied the trench width from 500 nm up to 3 μm while we kept the trench depth constant at 3 μm.
To simulate transport properties occurring in three-terminal MOS devices, a 50 nm thin insulating layer and a highly-doped-gate were added. The p-type doping concentration of our SiC-epi-layer was 10^{16} cm^{-3}. Dopant concentrations in the drain and source areas were a few orders of magnitude higher. For comparison, the parameters for the planar MOSFET were exactly the same except that the channel length was 3 μm. Fig. 5.2

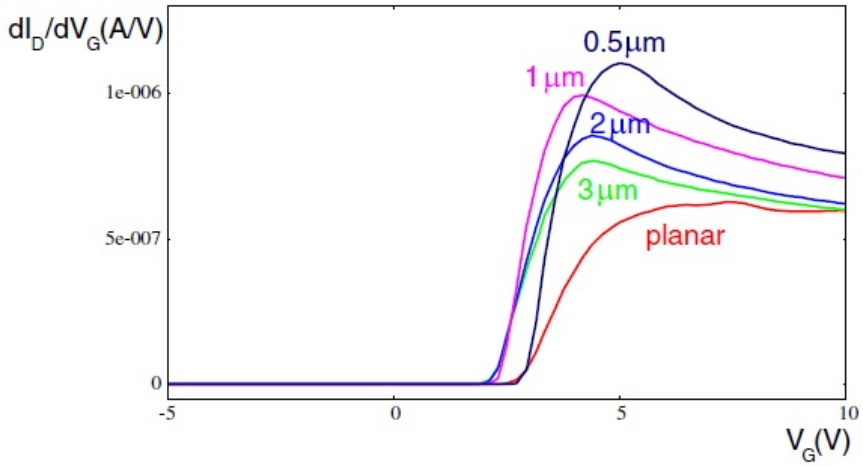

Figure 5.2: Comparison of simulated transconductance curves for different trench widths benchmarked against a planar SiC MOSFET with 3 μm channel length. Figure taken from [125].

shows the $\frac{dI_D}{dV_G} - V_G$ curves for different trench widths w_t = 500 nm, 1 μm, 2 μm and 3 μm. It can be seen that the transconductance of the devices clearly depends on the width of the structures and is found to be optimal for the smallest trench width of 500 nm. Furthermore, due to the lower oxide capacitance of thinner trench MOSFET designs the corresponding threshold voltage benefits by a shift towards higher gate voltages whose magnitude is comparable with current planar devices. Channel mobilities were found to increase for decreasing trench widths. Therefore, we may conclude that the power losses in the ON-state may be reduced by the utilization of a trench MOSFET architecture as compared to the planar devices. The origin of the better performance of the trenches is finally related to the physics of the channel mobility. The bulk mobility of 4H-SiC (0001) is 950 cm^2/Vs, but the channel mobility is drastically reduced due to a number of scattering mechanisms [138] at the 4H-SiC/insulator interface. Previous investigations of planar MOSFETs have yielded parameters of these scattering mechanisms [139]. The mobility of SiC-MOSFETs is reduced by impurity scattering, as well as by acoustic

phonon scattering and by a high surface roughness. The scattering due to impurities contributes only to a relatively small extent because of the low dopant concentration of 10^{16} cm^{-3} in the epitaxial layer. Scattering contributions due to acoustic phonons and surface roughness depend on the electrical field component perpendicular to the 4H-SiC/insulator interface. As shown in Fig. 5.3 it is found that the trenches, as compared

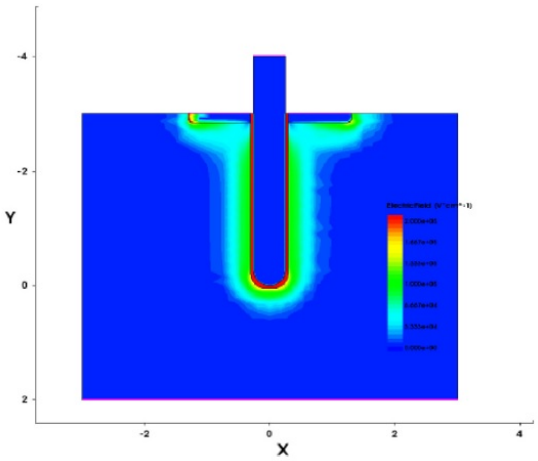

Figure 5.3: Electric field distribution for the 500 nm wide trench at 6.3 V gate voltage. At the corners of the source and drain well and the trench the electric field gets reduced compared to a more homogeneous field distribution for planar devices. The unit of the x-axis and the y-axis is μm. Figure taken from [125].

to planar devices, lead to reduced electrical fields in the vicinity of the drain and source regions, which lead to an improvement of the channel mobility and transconduction as determined by our numerical simulations. In a second step we investigated, again by

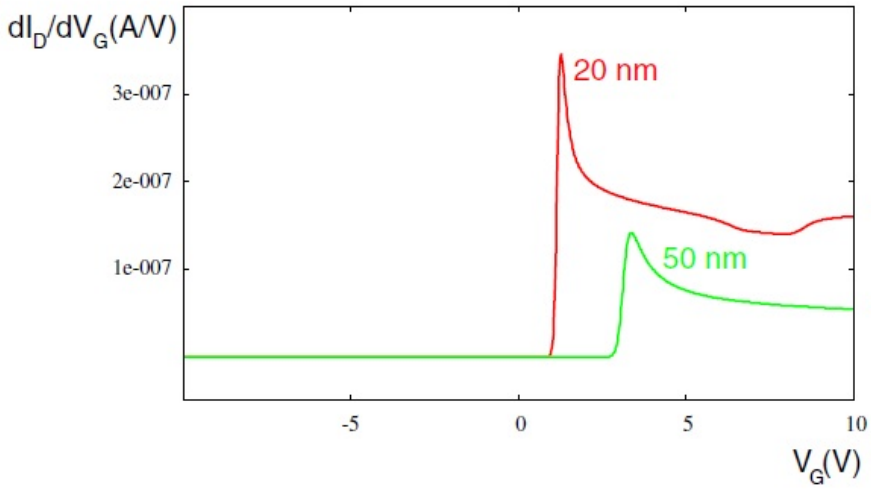

Figure 5.4: Comparison of simulated transconductance curves for different insulator thicknesses for the 500 nm wide trench. Figure taken from [125].

means of numerical simulations, the influence of the thickness of the gate insulator which we primarily set to 50 nm. As shown in Fig. 5.4, a reduction in the insulator thickness to 20 nm is decreasing the threshold voltage while at the same time the channel-mobility stays almost constant. The higher maximum value of the transconductance curve for the smaller insulator thickness suggests lower switching losses but could also lead to a premature breakdown of the device.

5.1.2 Dry-etching of trenched MOS-controlled FETs

For inductively-coupled plasma (ICP) etching of targeted 3 μm deep trenches in 4H-SiC special test structures for chip sizes of 10 mm $\times$ 11 mm have been designed and produced by electron-beam lithography. As a hard mask material Chromium (Cr) has been chosen since it can be easily deposited by electron-beam evaporation and since it offers a high enough selectivity to etch 3 μm deep trenches for our process. The fabrication consisted of the following process sequence: Electron-beam evaporation of 100 nm of Cr, spin coating of 270 nm PMMA (950 k 4%) on top of the hard mask, electron-beam writing of the trench test structures into the PMMA layer, PMMA development, selective opening of the Cr hard mask by a reactive ion-etching (RIE) process using a plasma consisting of a Cl_2/O_2 gas mixture. As a starting point for the ICP dry-etching process a SF_6-based

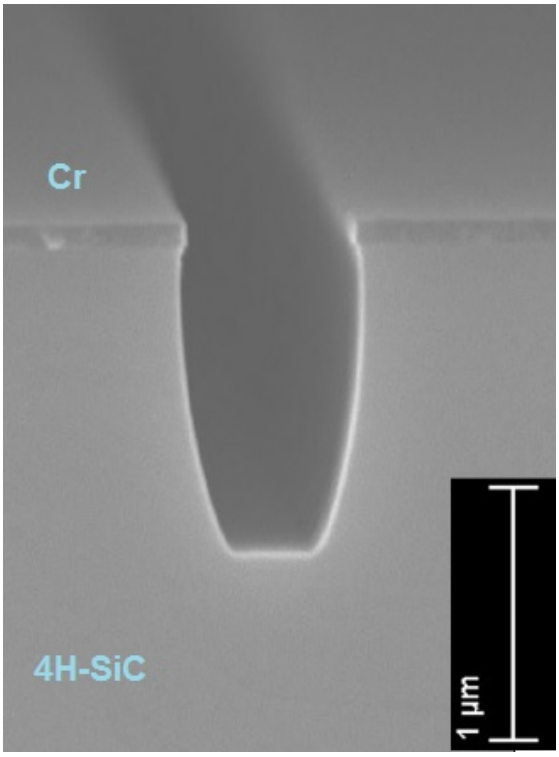

Figure 5.5: Cross section of the etched trench profile of the 0.5 μm wide trench as imaged by SEM. Figure taken from [125].

standard recipe [140] has been used and optimized according to [75, 141]. Our process is capable of etching high aspect ratio trenches into 4H-SiC with nearly vertical sidewalls and without trenching effects at the bottom of the trench (Fig. 5.5). Nevertheless, the etching rate still needs further adjustments to precisely etch 3 μm deep trenches. As shown in Fig. 5.6 the R_a roughness value at the bottom of these trenches which

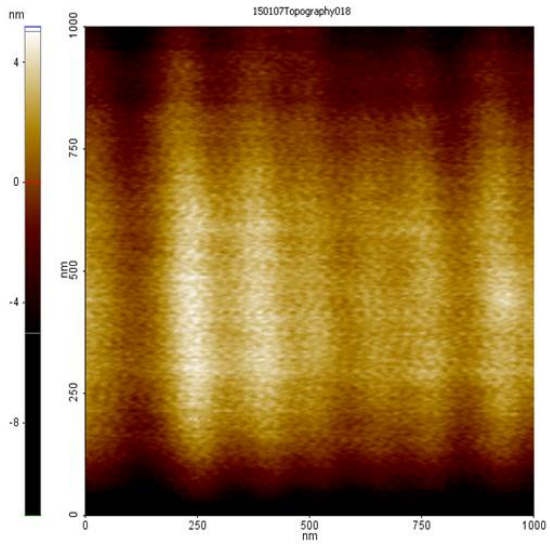

Figure 5.6: Roughness investigation at the bottom of one 3 μm wide trench with a scan area of 1 μm^2. The R_a roughness value was found to be 2.0 nm. Figure taken from [125].

we assume to be comparable to the sidewall roughness was evaluated by atomic force microscopy and found to be 2.0 nm. This value suggests that the profile quality of our trenches is sufficient to continue with the next processing steps since a damage removal treatment is expected to decrease the roughness even further [142].

5.1.3 Conclusions

Our numerical simulations clearly demonstrate that the trench MOSFET device architecture is able to outperform planar designs in terms of higher channel mobilities and smaller cell-pitch. This effect can be attributed to the lower electric field perpendicular to the 4H-SiC/insulator interface which leads to a suppression of the scattering processes induced by acoustic phonons and by a rough surface. Furthermore, the influence of the gate insulator thickness was studied with the conclusion that a thinner insulator is decreasing the threshold voltage even further while maintaining a high channel-mobility. The higher maximal tranconductance value of the 20 nm thick insulator diminishes switching losses but could also lead to a premature breakdown of the device.
Regarding the fabrication, we have shown that Cr is suitable as a hard mask material to etch high aspect ratio trenches. Additionally our process is capable to reach almost

perfect vertical sidewalls which support high mobilities. Furthermore, trenching effects at the bottom of the trench could be eliminated by the optimization of the plasma discharge conditions. Nevertheless, further experiments to precisely determine the etching rate still have to be performed.

CHAPTER 6

Summary and outlook

This thesis provides a detailed description of two fundamental aspects of semiconductor technology, namely the characterization of electronically active dopant profiles which determine the final device performance and the fabrication of power MOSFETs in SiC, whose wide band gap is offering superior power handling capabilities as compared to Si. Since the basic process flow of state of the art semiconductor devices requires various processing steps until the final device is manufactured powerful metrology tools are urgently needed to monitor the dopant architecture after each step and to ensure the desired device functionality at the end of the whole manufacturing cycle. Therefore it can be understood that these two topics are strongly correlated even though the two projects have been independently initiated in the beginning.

Within the following paragraphs a review on the past four years of my PhD work that was conducted at the Paul Scherrer Institute within the Laboratory for Micro- and Nanotechnology will be given. Therefore the initial goals of each project project, the achievements and the importance of these results for the corresponding community will be summarized.

In the second part the work that is still ongoing as well as possible continuation strategies will be discussed by the means of the acquired knowledge within this work and of the whole research area.

6.1 Achievements

The goal of the first project that is within the scope of this thesis was to address the capabilities of SPM-based microscopy methods in terms of the quantification of electronically active dopant profiles. At the initial stage the scientific community recognized the importance of characterization tools with a high spatial resolution that are able to quantitatively assess informations on carrier and dopant profiles. The driving force behind this development however was given by the ongoing miniaturization of devices. Here the main focus was different since two dimensional electrical characterization tools were needed especially in areas where the assessment by C-V measurements of entire layers was not sufficient anymore and on the other hand the sensitivity of carrier profiling methods to the low dopant regime was investigated. The latter is of utmost important for lightly doped drift layers in power devices that are needed to sustain high reverse voltages without a premature breakdown of the device. For the assessment of the sensitivity of SPM-based methods special Si test structures were beforehand manufactured in a similar way as Si Super-junction MOSFETs. Instead of the different terminals that are present at the wafer surface in a real MOSFET these test structures have been complemented by calibration layers that were well-characterized by C-V measurements and later on used to gauge the acquired SPM signals.
From a material perspective Si was chosen to start with since it is still the most widely used substrate even for power applications. The extension towards wide band gap materials however was planned from the beginning. Among other things this was one of the main reasons to develop a polishing procedure since SiC can not be cleaved in a very controllable manner. Further a waste of the at this time costlier material should be prevented. The focus on lightly doped layers was also driven by SiC since the intrinsic carrier concentration is much lower than in Si and therefore a higher sensitivity for this material is needed. Last but not least an explanation why the focus in this work is given to carrier and not dopant profiling techniques can be found by looking at the different ionization energies of donor/acceptor atoms in SiC. Holes are tightly bound and therefore not all acceptors are ionized after the activation annealing. The discrepancy between the carrier and the dopant profile in this case can be sufficient to cause a malfunctioning of the device.
As mentioned above one of the first achievements was the establishment of a reproducible cross-section preparation routine that ensures a low surface state density and therefore enables KPFM measurements. If this would not be the case the Fermi level would be pinned to defect states and the quantification possibilities of this method would completely vanish. On this basis the comparison of three different SPM based methods, namely KPFM, SCFM and SSRM has been performed within the same custom built AFM equipment. This has been a clear advancement as compared to previous studies

since so far different methods were compared between different laboratories and also on the basis of different calibration samples. Further the same parameters of the sample preparation routine could not be guaranteed. Within the here presented analysis it was found that different information depths can be mapped depending on the underlying physical contrast mechanism of each method. Based on this investigation it can be concluded that the only reliable quantitative results can be gained by SSRM measurements since for KPFM the high surface sensitivity of this method is prone to surface depletion effects. SCFM on the other hand shows a high sensitivity for lightly doped layers and the extended depletion capacitance is averaging out surface effects. The shape of the corresponding spectroscopy curves however is not yet well understood. The often mentioned disadvantage of SSRM, namely the destructive operation in contact mode, was actually found to be key for a reliable quantification procedure due to the additional self-preparation of the surface during the measurement. Notably, also the non-contact measurements were performed on the cross-section of a dedicated specimen which requires a 'destruction' of the device.

These findings were a high enough motivation to study the potential of SSRM in more detail. Three possible methods for quantifying the carrier concentration inside the p-pillars of Super-junctions have been identified and discussed within this work. One method is based on the variation of the width of the SCR under forward and reverse biasing the tip-sample junction. An other approach that has not been addressed so far was the consideration of a dopant and temperature dependent mobility model for fitting the experimental data of the calibration layers. Especially for dopant concentrations around $N_{A,D} = 10^{17}$ cm^{-3} the mobility is far away from being constant and instead shows large variations with an increase or decrease of the concentration. Further, the nature of the tip-sample contact has been studied by I-V measurements. A Schottky contact behaviour was observed and a clear differentiation of the resulting I-V curves for each concentration was possible. These data sets were fitted by an extended thermoionic emission model which takes also a shunt resistance into account. The extracted fit parameters were showing reasonable trends however the quantification potential by the dopant dependent barrier lowering contribution still needs further investigation.

Simultaneously to the above described developments these concepts have been extended to SiC where two technologically relevant problems have been analysed. One of them is the characterization of epitaxially grown n-type 4H-SiC layers while the other one is the imaging of a p-doped shielding structure of a Schottky barrier diode. It was found that resolution at the boundaries between differently doped n-type regions is blurred out due to the presence of surface defects that cause band bending effects. The application of a surface photo voltage which gets established under laser illumination of the sample was able to diminish this effect. This is due to the fact electron-hole pairs are generated within the semiconductor that can diffuse towards the surface and passivate those defect

states. Hence this analysis method is a suitable tool to characterize the sharpness of the junction between differently doped epitaxial layers. For the shielding structures present below the Schottky contact the EFM based methods revealed more details as compared to SEPC measurements.

The second project that is covered within the scope of this thesis was related to the fabrication of lateral trench MOSFETs in 4H-SiC. Notably, the structure is very similar to vertical power devices that have been already fabricated and characterized. The novelty of the here presented structure lies in the fact that the channel resistance can be precisely addressed. Especially in the medium power range the ON-state resistance contribution of the channel is quite significant while in the high power regime the resistance contribution of the drift region is dominant. In the initial stage of this project focus was given to device simulations to determine the optimal trench geometry in terms of a high channel mobility. In parallel ICP etch tests on small chips have been performed to determine the optimal etching parameters for the desired trench structures. This has been done in an iterative trial and error manner that was backed up by the few available literature reports. After the optimization of this challenging process the whole process flow with the corresponding mask layouts has been designed. Based on this design the ion implantation step was carried out by a subcontractor and in parallel first MOS Capacitors have been fabricated. The challenging oxidation step as well as the necessity of additional outsourced processes however lead to the fact that work towards a full trench MOSFET is still ongoing.

6.2 Ongoing and future work

Regarding the dopant imaging project further investigations on the SSRM quantification procedure are still ongoing. Most recent results according to the I-V measurements have shown a Schottky contact behaviour. In contrast the fit of the experimental data that is based on the Arora mobility model was taking only an ohmic contact into account. Therefore this model needs to be extended accordingly. Further, due to the low dopant concentration inside the trench new calibration structures have to be fabricated where the lowest doping level of one of the calibration layers has to be below the doping concentration inside the trench.
Once these challenges are overcome one can think of the visualization of dopant profiles and the corresponding space charge regions during the operation of the device as it has been done for SCM measurements [143]. These kind of measurements on one hand would need a proper contact patterning of the backside contact and of the contacts where the voltage is applied to the device. On the other hand a modification of the AFM system is required. Problems regarding the ageing of devices could in this way be systematically studied. From this possibility the device failure analysis would benefit since to the best of my knowledge this is nowadays only done after the device is fully broken after numerous load and unload cycles. However it is speculated that modifications of the dopant profile occur beforehand. Therefore new insights in terms of a reliable device design can be gathered.
Regarding the second project preliminary results suggested that the thermal oxide growth on 4H-SiC is limited due to the maximum operating temperature of our oxidation furnace of 1050 °C. Due to the presence of C atoms the oxidation process is showing a higher complexity and the subsequent passivation mechanisms to neutralize the effect of interface trap states are not yet well understood. In the case of trench devices it also has to be considered that a thermally grown oxide is anisotropic. For a Si-face substrate as it was used here this would result in a higher oxide thickness at the trench sidewalls as compared to the trench bottom. The highest electric fields when the device is operated in reverse direction however is expected to built up at the horizontal interface at the trench bottom. Therefore in our configuration this anisotropy would result in a lower voltage class of the device. Hence, high k-materials with a larger dielectric constant that can be conformally deposited by Atomic Layer Deposition (ALD) are promising candidates as gate insulators. Furthermore, high-k gate dielectrics induce a lower electric field inside the thin conducting channel that is formed when the gate voltage exceeds the threshold voltage. This allows fore a more reliable gate operation at lower gate voltages since the threshold voltage is shifted to lower values due to the higher gate capacitance as compared to SiO_2. The unfavourable effect of a high dielectric constant on the mobility gets compensated by a higher transconductance. Potential im-

provements have already been demonstrated in planar devices [144, 145] and the logical next step is to use this technology also for trench MOSFETs. The addition of a nitrogen conditioning step [146] before the ALD deposition of the gate insulator is expected to produce a high quality surface in terms of a low roughness and a low density of interface states. Hence the combination of these two concepts might enable a new class of high energy efficient power MOSFETs.

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Acknowledgments

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Publication list

The following chapter summarizes the scientific achievements that were accomplished during the course of my projects and organizes the results in lists corresponding to the way how they were presented.

Scientific articles:

1. H. R. Rossmann, U. Gysin, A. Bubendorf, T. Glatzel, S. Reshanov, A. Schöner, T. A. Jung, E. Meyer and H. Bartolf, "Two-Dimensional Carrier Profiling on Lightly Doped n-Type 4H-SiC Epitaxially Grown Layers", *Materials Science Forum* **821-823**, 269 (2015).

2. H. Bartolf, U. Gysin, T. Glatzel, H. R. Rossmann, T. A. Jung, S. Reshanov, A. Schöner and E. Meyer, "Improving the Design of the Shield for the Electric Field in SiC-Based Schottky-Rectifiers and Ion-Implantation Cascades by SPM Dopant-Imaging", *Microelectronic Engineering* **148**, 1 (2015).

3. H. R. Rossmann, A. Bubendorf, F. Zanella, N. Marjanovic, M. Schnieper, E. Meyer, T. A. Jung, J. Gobrecht, R. Minamisawa and H. Bartolf, "Device Simulations on Novel High Channel Mobility 4H-SiC Trench MOSFETs and Their Fabrication Processes", *Microelectronic Engineering* **145**, 166 (2015).

4. H. Bartolf, U. Gysin, H. R. Rossmann, A. Bubendorf, T. Glatzel, T. A. Jung, E. Meyer, M. Zimmermann, S. Reshanov and A. Schöner, "Development of power

semiconductors by quantitative nanoscale dopant imaging", *Proceedings of the 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 281 (2015).

5. U. Gysin, E. Meyer, T. Glatzel, G. Günzburger, H. R. Rossmann, T. A. Jung, S. Reshanov, A. Schöner and H. Bartolf, "Dopant imaging of power semiconductor device cross sections", *Microelectronic Engineering* **160**, 18 (2016).

6. H. R. Rossmann, U. Gysin, A. Bubendorf, T. Glatzel, S. Reshanov, A. Zhang, A. Schöner, T. A. Jung, E. Meyer and H. Bartolf, "Junction Barrier Schottky (JBS) Rectifier Interface Engineering Facilitated by Two-Dimensional (2D) Dopant Imaging", *Materials Science Forum* **858**, 497 (2016).

7. J. Girovsky, J. Nowakowski, Md. Ehesan Ali, M. Baljozovic,H. R. Rossmann, T. Nijs, E. Aeby, S. Nowakowska, D. Siewert, G. Srivastava, C. Wäckerlin, J. Dreiser, S. Decurtins, Shi-Xia Liu, P. M. Oppeneer, T. A. Jung and N. Ballav, "Long-range ferrimagnetic order in a two-dimensional supramolecular Kondo lattice", submitted to *Nature Materials*, (2016).

8. H. R. Rossmann *et al.* "Quantitative Dopant Imaging, Spectroscopy and Space Charge Region Observation by SSRM on Semiconductor Device Cross-Sections", *in preparation* (2016).

Conference contributions:

Oral presentations

1. H. R. Rossmann, U. Gysin, A. Bubendorf, T. Glatzel, H. Bartolf, T. A. Jung and E. Meyer, "Two-dimensional dopant concentration imaging by means of scanning probe microscopy techniques", *LMN Science talk*, Villigen, Switzerland, August 29$^{\text{th}}$, 2013

2. H. R. Rossmann, U. Gysin, A. Bubendorf, T. Glatzel, H. Bartolf, T. A. Jung and E. Meyer, "Electronically active dopant profiling of power semiconductor structures by complementary Scanning Probe Microscopy (SPM) techniques", *SLS Symposium on Imaging*, Villigen, Switzerland, June 8$^{\text{th}}$, 2014

3. H. R. Rossmann, U. Gysin, A. Bubendorf, T. Glatzel, S. Reshanov, A. Schöner, T. A. Jung, E. Meyer and H. Bartolf, "Two-Dimensional Carrier Profiling on Lightly Doped n-type 4H-SiC Epitaxially Grown Layers", *European Conference on Silicon Carbide and Related Materials (ECSCRM)*, Grenoble, France, September 21$^{\text{st}}$-25$^{\text{th}}$, 2014

4. H. R. Rossmann, A. Bubendorf, U. Gysin, T. Glatzel, F. Zanella, N. Marjanovic, M. Schnieper, H. Bartolf, R. Minamisawa, E. Meyer, T. A. Jung and J. Gobrecht, "Characterization and fabrication of high mobility nanoscale trench MOSFETs in 4H-SiC", *LMN Science talk*, Villigen, Switzerland, March 12$^{\text{th}}$, 2015

5. H. R. Rossmann, A. Bubendorf, F. Zanella, N. Marjanovic, M. Schnieper, E. Meyer, T. A. Jung, J. Gobrecht,R. Minamisawa and H. Bartolf, "On the Assessment of Channel Mobilities in 4H-SiC Trench MOSFETs", *SNI Annual meeting*, Lenzerheide, Switzerland, September 3$^{\text{rd}}$-4$^{\text{th}}$, 2015

Poster presentations

1. H. R. Rossmann, U. Gysin, A. Bubendorf, H. Bartolf , T. A. Jung, T. Glatzel and E. Meyer, "Analysis of power semiconductor diodes by the means of Scanning Probe Microscopy", *Nanotechnology for SME: Funding opportunities and collaborations with universities*, Windisch, Switzerland, November 22$^{\text{nd}}$, 2012

2. U. Gysin, H. R. Rossmann, A. Bubendorf, H. Bartolf , T. A. Jung, T. Glatzel and E. Meyer, "Dopant Concentration Imaging by Means of Scanning Probe Microscopy Methods", *Swiss Nano Convention (SNC)*, Basel, Switzerland, May 23$^{\text{rd}}$-24$^{\text{th}}$, 2013

3. H. R. Rossmann, U. Gysin, A. Bubendorf, T. Glatzel, H. Bartolf , T. A. Jung, and E. Meyer, "Towards ultra-low dopant concentration carrier profiling and quantification by complementary Scanning Probe Microscopy (SPM) techniques", *5th International Workshop on Advanced Scanning Probe Microscopy Techniques (ASXMT)*, Karlsruhe, Germany, February 24$^{\text{th}}$-25$^{\text{th}}$, 2014

4. U. Gysin, T. Glatzel, E. Meyer, H. R. Rossmann, T. A. Jung and H. Bartolf, "Dopant imaging of Si and SiC structures using different SPM methods", *Swiss Nano Convention (SNC)*, Brugg-Windisch, Switzerland, May 21$^{\text{st}}$-22$^{\text{nd}}$, 2014

5. H. R. Rossmann, F. Zanella, N. Marjanovic, M. Schnieper, T. A. Jung, E. Meyer, J. Gobrecht, R. Minamisawa and H. Bartolf, "Device simulation and fabrication of novel 4H-SiC nano trench MOSFET devices", *Swiss Nano Convention (SNC)*, Brugg-Windisch, Switzerland, May 21$^{\text{st}}$-22$^{\text{nd}}$, 2014

6. H. R. Rossmann, F. Zanella, N. Marjanovic, M. Schnieper, T. A. Jung, E. Meyer, J. Gobrecht, R. Minamisawa and H. Bartolf, "Device simulations and fabrication processes of novel 4H-SiC nano trench MOSFETs", *SNI Annual meeting*, Lenzerheide, Switzerland, September 11$^{\text{th}}$-12$^{\text{th}}$, 2014

7. U. Gysin, T. Glatzel, H. R. Rossmann, T. A. Jung, E. Meyer, S. Reshanov, A. Schöner and H. Bartolf, "Designing the Shield for the Electric Field in High-Voltage SiC-Based Schottky-Rectifiers by Ion-Implantation and SPM Dopant-Imaging", *40th Int. Micro and Nano Engineering Conference (MNE)*, Lausanne, Switzerland,

September 22nd-26th, 2014

8. H. R. Rossmann,C. Wäckerlin, J. Nowakowski, Shi-Xia Liu, M. Jaggi, J. Girovsky, D. Siewert, A. Wäckerlin, M. Baljozovic, A. Kleibert, P. M. Oppeneer, F. Nolting, S. Decurtins, T. A. Jung and N. Ballav, "Chemically programmable 2D electron spin array", *Spinmol Conference 2014*, Ascona, Switzerland, October 26th-30th, 2014

9. H. Bartolf, H. R. Rossmann, A. Bubendorf, U. Gysin, T. Glatzel, T. A. Jung, E. Meyer, M. Zimmermann, S. Reshanov and A. Schöner, "Development of Power Semiconductors by Quantitative Nanoscale Dopant Imaging", *27th International Symposium on Power Semiconductor Devices and ICs 2015 (ISPSD)*, Hong-Kong, China, May 11th-14th, 2015

10. H. R. Rossmann, A. Bubendorf, F. Zanella, N. Marjanovic, M. Schnieper, T. A. Jung, E. Meyer, J. Gobrecht, R. Minamisawa and H. Bartolf, "Numerical Simulations on Novel High Channel Mobility 4H-SiC U-MOSFET Devices and their Fabrication", *Swiss Nano Convention (SNC)*, Neuchatel, Switzerland, May 27th-28th, 2015

11. H. R. Rossmann, D. Dutta, S. Goedecker, L. Zhu, S. Roy, A. Bubendorf, F. Zanella, N. Marjanovic, M. Schnieper, E. Meyer, T. A. Jung, J Gobrecht, R. Minamisawa, J. Lehmann, H. Bartolf, A. Schöner and S. Gerstl, "Novel High Channel Mobility SiC- MOSFET Devices and their Fabrication", *i-net Nano Technology Event «Innovation Landscape Nano»*, Muttenz, Switzerland, September 9th, 2015

12. H. R. Rossmann, U. Gysin, A. Bubendorf, T. Glatzel, H. Bartolf , T. A. Jung, and E. Meyer, "Power Semiconductor Device Development Facilitated by Dopant Imaging on the Nanometer Scale", *i-net Nano Technology Event «Innovation Landscape Nano»*, Muttenz, Switzerland, September 9th, 2015

13. H. R. Rossmann, U. Gysin, A. Bubendorf, T. Glatzel, S. Reshanov, A. Zhang, A. Schöner, T. A. Jung, E. Meyer and H. Bartolf, "Junction Barrier Schottky (JBS) Rectifier Interface Engineering Facilitated by Two-Dimensional (2D) Dopant Imaging", *International Conference on Silicon Carbide and Related Materials (ICSCRM)*, Giardini Naxos, Italy, October 4th-9th, 2015

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