Nano Field Effect Transistors as basic building blocks for sensing

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It is the glory of God to conceal a thing:
but the honour of kings is to search out a matter.

King Solomon, Proverbs 25: 2

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CHAPTER 1

Introduction

1.1 Motivation

Chemical and biological sensing are old fields but of increasing interest. The goal of any chemical or biological sensing scheme is to detect a particular molecule. This is done by monitoring a specific binding or reaction between the molecules of interest — the so called analyte — and a well known recognizing molecule. In nondestructive analysis methods this is done by making use of physical properties of this bound pair or new product. Examples of such techniques are optical spectroscopy, chromatography, mass spectroscopy or precipitation. Today's demand is not only for detecting one specific analyte, but more and more for systematic analysis. Therefore the integration of a huge amount of analysis tools into an automatized process is required. Industry and basic science could both

profit from such systems. Ideas range from automatized health monitoring in medicine to most detailed analysis of complex biological systems in systems-biology. Traditional analysis techniques hardly can meet the requirements of such an integration. Simple interfaces to computerized aquisition and controlling systems and minituarization are key factors. In computer industry a breakthrough was the step from fabricating and combining individual transistors to integrated chips where a complete system is fabricated at once. In analogy to this one would like to fabricate a complete bio-chemical lab integrated in combination with microfluidics onto a single chip. Such a device is simply called Lab-On-Chip.

To implement sensors in such a Lab-On-Chip an interface is needed to transduce a chemical binding event into an electronic signal. In this context it is naturally to study the response of semiconductors to their chemical environment. At the surface of a semiconductor, charges can be induced by the local electrical potential of nearby molecules. Such charges influence the conductance of the semiconductor. Changes in its conductance can easily be measured by contacting the semiconductor to an electronic setup. By a third electrode — the gate electrode — an electric field can be applied to induce extra charges. This way we have a Field Effect Transistor (FET) where the current for fixed bias voltage can be controlled by a gate electrode on one hand and on the other hand by charges of chemical species at the semiconductor surface.

Requirements for FETs are different in this context than in the context of computing by logic switching. The semiconductor as sensitive part has to be exposed to the media of interest. It has to be small but with high surface area as sensing is a surface effect. To be more precise the ratio between surface charges and the total number of current carrying charges has to be high. For many Lab-On-Chip applications sensitivity to a small amount of analyte molecules is desired.

1.2 About this work

Ideal candidates for such FETs are Silicon Nanowire FETs and Carbon Nanotube FETs. The two are investigated experimentally in this work.

For both types of devices, pioneering sensing assays have been reported (see Section 5.1.2 for a small literature review). Here we focus on an improved control over device fabrication and performance.

In Chapter 2 the working principle of conventional MOSFETs is introduced and silicon nanowire FETs are described as a special case of MOSFETs. To describe carbon nanotube FETs a small model is presented based on the MOSFET theory.

The design and fabrication of the two types of nano FETs is described in Chapter 3. General design and process considerations are discussed as well as fabrication details.

Chapter 4 elaborates the FET behavior of the silicon nanowire and carbon nanotube FETs.

The potential for sensing application of silicon nanowire and carbon nanotube FETs is discussed in Chapter 5. It begins with an introduction in MOSFET based chemical and biological sensing. The study of silicon nanowire FETs in liquid environment shows pH sensitivity and that good control of the hole system is mandatory. For carbon nanotube FETs the extremely high sensitivity is shown as well as challenges in reliability.

A comparison of the two systems in Chapter 6 summarizes and concludes this work.

CHAPTER 2

Theoretical background

2.1 Standard FET theory

This Section gives a short introduction to standard Field effect Transistor theory. It is intended for readers that are not familiar with the terminology and working principle of FET devices. Readers who are interested in more details should consult a standard textbook on semiconductor devices as the well known book from Sze [1] or the online book from Van Zeghbroeck [2].

The geometry of a standard Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is shown in Figure 2.1 (a). Two highly n-doped contact regions are separated by the low p-doped substrate. Because of the two p-n junctions no current can flow, even if a bias is applied between source and drain contacts. At the surface of the semiconductor, between the

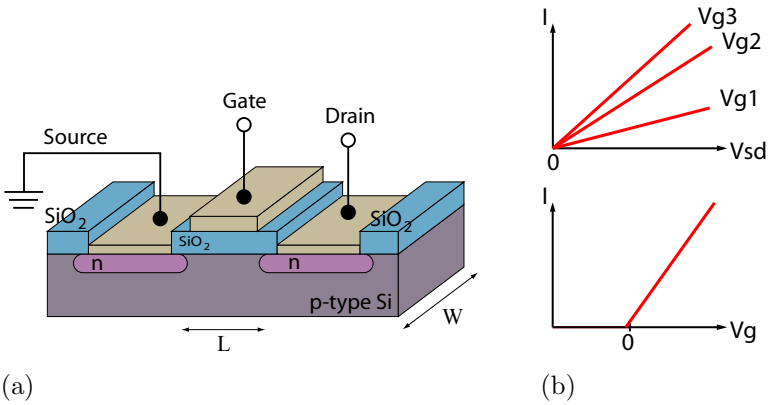


Figure 2.1: (a) Schematics of a MOSFET. (b) Simplified current vs. bias (top) and gate voltage (bottom) characteristics.

contact regions, there is a metal gate electrode separated by an insulating oxide layer. Electrons can be induced at the semiconductor–oxide interface when a positive voltage is applied to the gate. In this case a current flows. In a linear model it is proportional to the amount of induced electrons. In Figure 2.1(b) the current is sketched as function of a voltage applied between source and drain V_{sd} and a voltage applied to the metal gate V_g. As long as the bias applied between source and drain is not too high, the current density can be described by Ohms law

$$\vec{j} = \sigma \vec{E}, \qquad j = \sigma \frac{V_{sd}}{L}$$

where $|\vec{E}| = V_{sd}/L$ is the applied electric field with the source - drain bias V_{sd} and L the length of the separation between the contact regions. The conductivity σ is given by the Drude model as $\sigma = en\mu$ with the carrier mobility μ and the carrier concentration n [3].

To deduce the carrier concentration n we look at the capacitor made up of the metal gate, oxide insulator and the semiconductor. In a first step, we

assume it to behave as a perfect plate capacitor not depending on applied voltages. The induced charge is given by the product $Q = C_g \cdot V_g$ of the capacitance C_g and the applied gate voltage V_g. The charge density follows as $en = C_g' V_g / h_s$ with the height of the charge carrier sheet h_s and the capacitance per unit area $C' = C/(W \cdot L)$. Assuming that the mobility and the gate capacitance C_g are independent of the applied voltages and assuming no intrinsic charges, the current is given by

$$I = W h_s j = W h_s e \mu n \frac{V_{sd}}{L} = \frac{W}{L} \mu C_g' V_g V_{sd}. \tag{2.1}$$

This is the most basic transistor relation. The way it has to be modified when the above assumptions are generalized depends on the specific system. We have to treat MOSFETs, nanowire FETs and carbon nanotube FETs separately. The case of MOSFETs is briefly discussed first. In Section 2.2 modifications for the case of nanowire FETs are explained. Nanotube FETs are discussed in Section 2.3 following the same line as the discussion below.

2.1.1 MOS capacitor terminology

First we discuss the metal oxide semiconductor (MOS) capacitor shown in Figure 2.2. We discuss the situation of a p-type semiconductor. When applying a negative voltage on the gate electrode, holes are accumulated in the semiconductor. These holes are at the interface to the oxide within a thin layer, the so-called accumulation layer. When a positive voltage is applied, the intrinsic holes have to be depleted. In the depletion region, there are no mobile charges, but only the immobile acceptor ions. To simplify, the depletion approximation is used which assumes that the depleted charge Q_d has a box profile of width W_d as sketched in Figure 2.2. Thus $Q_d = -eN_aW_d$ with the acceptor dopant density N_a and the elementary charge e. When the gate voltage is driven further, electrons are induced at the interface. They build up the inversion charge Q_{inv} in the thin inversion layer of width W_{inv}.

The transfer from accumulation to depletion region occurs at finite voltage V_{fb} called flat band voltage. It is the voltage at which the bands in the

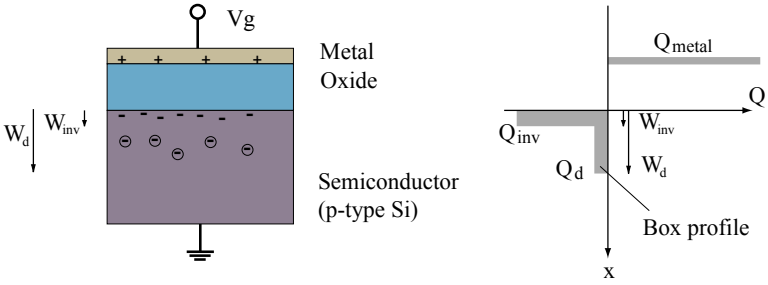


Figure 2.2: Metal Oxide Semiconductor (MOS) structure in inversion regime.

semiconductor are flat all the way from the bulk to the oxide interface as shown on the left side of Figure 2.3. In the ideal case the flat band voltage is given by difference in work function of the metal ϕ_m and the silicon ϕ_s: $V_{fb} = \phi_m - \phi_s$. In real devices one has to consider charges within the oxide Q_{ox}. They contribute via the gate capacitance C_g so that the total flat band voltage is given by

$$V_{fb} = \phi_m - \phi_s - \frac{Q_{ox}}{C_g}. \tag{2.2}$$

The potential difference between the Fermi energy and the middle of the band gap is given by Ψ_B as sketched in Figure 2.3. If a voltage different than the flat band voltage is applied on the gate, the bands are bent towards the interface. The potential at the interface with respect to the intrinsic energy level E_i is called Ψ_s (Figure 2.3 right). It is defined to be positive when the bands bend downwards. In the bulk of the semiconductor the bands are not affected. There the potential Ψ_B remains, and therefore it is called "bulk potential". With these definitions we have a measure for the different regimes mentioned in the previous paragraph. We have:

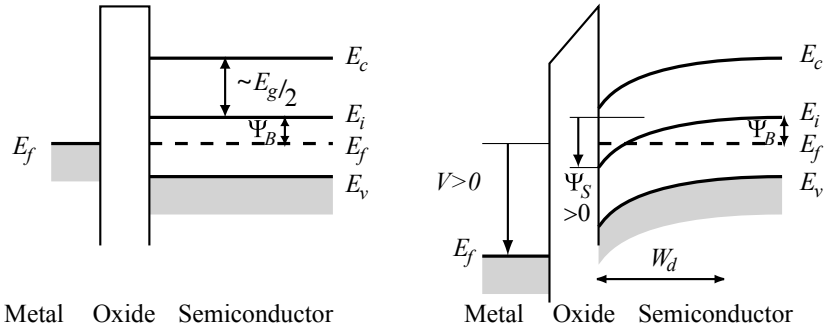


Figure 2.3: Band bending in MOS structure for p-type semiconductor in flat band condition (left) and in weak inversion (right). Energies are indicated for conduction band E_c, valence band E_v, band gap E_g, intrinsic energy (mid-band) E_i and Fermi energy E_f.

$\Psi_s < 0$	Accumulation of holes
$\Psi_s = 0$	Flat band condition
$0 < \Psi_s < \Psi_B$	Depletion of holes
$\Psi_s = \Psi_B$	Fermi level at midgap, at interface $n = p$
$\Psi_B < \Psi_s < 2\Psi_B$	Weak inversion, at interface $n > p$
$2\Psi_B < \Psi_s$	Strong inversion, at interface $n > N_a$

2.1.2 Surface depletion

Depletion at the semiconductor surface occurs whenever the surface potential $\Psi_s > 0$. In a MOS structure this might be caused by a gate voltage. In general, at any semiconductor surface, the potential can be shifted by surface charges or surface states. Such surface states can come from perturbation of the bulk band structure at the interface [4, 5].

In a doped semiconductor free carriers can fill these surface states which leads to a surface charge n_s and an oppositely charged depletion region below the surface that can be more extended. We look at the case of

p-type semiconductor with acceptor concentration N_a. In the depletion region all acceptors are ionized giving a space charge density of $-eN_a$ and a total depletion region charge of $-eN_aW_d$. The potential is described by the Poisson equation

$$\frac{d^2\Psi}{dx^2} = \frac{eN_a}{\varepsilon_r\varepsilon_0} \Rightarrow \Psi = \frac{eN_a}{2\varepsilon_r\varepsilon_0}(x - W_d)^2. \tag{2.3}$$

The potential at the interface is given by the surface potential $\Psi(0) = \Psi_s$. With this we can get the depletion width:

$$W_d = \sqrt{\frac{2\varepsilon_r\varepsilon_0\Psi_s}{eN_a}}. \tag{2.4}$$

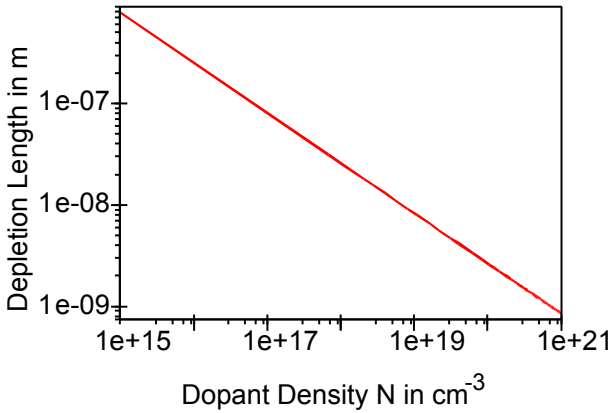


Figure 2.4: Depletion width as function of dopant density for silicon for surface potential $\Psi_s = E_g/2$.

In Figure 2.4 the depletion width is plotted as function of the dopant density of silicon. The surface potential is assumed to have the size of half the band gap $\Psi_s = E_g/2$.

2.1.3 MOS capacity

In a MOS capacitor the voltage applied on the gate partially drops across the insulator and partly within the semiconductor

$$V_g = V_i + V_s.$$

The voltage drop within the semiconductor corresponds to the surface potential Ψ_s and the voltage drop across the insulator is given by the charge Q_s on the semiconductor

$$V_i = |\vec{E}|d = \frac{Q_s/Ad}{\varepsilon_{SiO_2}\varepsilon_0} = \frac{Q_s}{C_{ox}}.$$

with the oxide capacitance $C_{ox} = A\varepsilon_{SiO_2}\varepsilon_0/d$ where d is the thickness of the oxide and A the area of the interface. With this the relation between the applied gate voltage and the surface potential is

$$V_g = \Psi_s + \frac{Q_s}{C_{ox}} \tag{2.5}$$

In MOSFETs the gate voltage that has to be applied to reach the onset of strong inversion is called threshold voltage

$$V_{th} = V_{fb} + 2\Psi_B + \frac{Q_s}{C_{ox}}. \tag{2.6}$$

The relation between the the surface potential and the induced charge can be described by the semiconductor capacitance $C_s = dQ_s/d\Psi_s$. This capacitance depends very much on type of system we are looking at (more details in Section 2.2). In case of a standard MOS capacitor, we can think of a depletion layer capacitance $C_d = dQ_s/d\Psi_s$. This capacitance depends on the applied voltage and on the frequency of charging. In depletion regime one can think of it as a plate capacitor with plates separated by the depletion width $C_d = A\varepsilon_{Si}\varepsilon_0/W_d$.

The total gate capacitance is the series capacitance of the oxide capacitance and the depletion capacitance

$$C_g^{-1} = C_{ox}^{-1} + C_d^{-1}.$$

In accumulation and strong inversion the depletion width goes to zero and the total gate capacitance C_g is dominated by C_{ox}.

2.1.4 Subthreshold regime

In depletion or weak inversion the electrostatics in the semiconductor is dominated by the charge of the immobile ions in the depletion region $-eN_aW_d$ as described in Section 2.1.1. But now we are interested in the small mobile charge that can be thermally excited in the depletion zone because this gives rise to a small subthreshold current. The carrier concentration far away from the Fermi energy is given by the Boltzmann distribution $n = n_i \exp(-e\Psi/kT)$ and so

$$Q = e\int_0^{W_d} n(x)dx = e\int_{\Psi_s}^{0} \frac{n(\Psi)}{d\Psi/dx}d\Psi = en_i\int_{\Psi_s}^{0} \frac{1}{d\Psi/dx}e^{-\frac{e\Psi}{kT}}d\Psi.$$

With $d\Psi/dx$ from Equation 2.3 the integral approximatively [6] gives

$$Q = kT\sqrt{\frac{\varepsilon_0\varepsilon_{Si}}{2e\Psi_s N_a}}\left(\frac{n_i}{N_a}\right)^2 e^{-e\Psi_s/kT}.$$

The square-root term is a much weaker function of Ψ_s compared to the exponential term and can be treated as constant [1]. Thus the mobile charge in the depletion region and with it the current in the subthreshold regime depend exponentially on the surface potential Ψ_s: $I \propto \exp(-e\Psi_s/kT)$. To relate this to the applied gate voltage we calculate $dV_g/d\Psi_s$ from Equation 2.5 including $C_d = dQ_s/d\Psi_s$:

$$\frac{dV_g}{d\Psi_s} = 1 + \frac{C_d}{C_{ox}}.$$

The subthreshold swing S is defined as the gate voltage change needed to suppress the subthreshold current by one order of magnitude:

$$\begin{aligned} S &= \left|\frac{dV_g}{d(\log(I))}\right| = \left|\ln(10)\frac{dV_g}{d(\ln(I))}\right| = \ln(10)\frac{dV_g}{e/kTd\Psi_s} \\ &= 59.6\,\mathrm{mV}\frac{kT}{e}\left(1 + \frac{C_d}{C_{ox}}\right). \end{aligned} \tag{2.7}$$

Interface trap states at the semiconductor – oxide interface lead to an extra capacitance per area $C'_{it} = e^2 D_{it}$ in parallel with the depletion layer capacitance per area $C'_d = C_d/A$ and $C'_{ox} = C_{ox}/A$. D_{it} is the density of interface traps per energy and area. The modified subthreshold swing is

$$S = \ln(10)\frac{kT}{e}\left(1 + \frac{C'_d + e^2 D_{it}}{C'_{ox}}\right). \tag{2.8}$$

With higher trap state density D_{it} the subthreshold slope is less sharp.

2.2 Nanowire FETs

In CMOS technology down-scaling is driven by the need of ever higher integration. The channel length L is pushed down further and further and with it the gate oxide thickness, applied voltages and device resistance. In contrast to this the channel length L of nanowire FETs and nanowire like structures is much larger than the channel width W. Short channel effects don't come into play as the gate insulator thickness d is smaller than the channel length L. But the diameter of the nanowire semiconductor body is now much smaller than the depletion width (see Figure 2.4). Therefore we have to reconsider the semiconductor capacitance. From equation 2.5 we get for the MOS structure $V_g = \Psi_s + |Q_s|/C_{ox}$. As the semiconductor body is too thin, the last term cannot be related to the depletion capacitance as we used to do for the standard MOS structure. We use a more general expression for the relation between the semiconductor charge and the surface potential $dQ_s/d\Psi_s = Aedn/d\Psi_s = C_s$ leading to the general semiconductor capacitance C_s. With this we get the relation

$$\frac{dV_g}{d\Psi_s} = 1 + \frac{C_s(\Psi_s)}{C_{ox}}. \tag{2.9}$$

Let's consider two special cases. If the gate oxide layer is much thicker than the charge layer in the semiconductor, we are in the regime of $C_{ox} \ll C_s$. In this case gate variations lead to

$$dV_g \approx d\Psi_s C_s/C_{ox} = edn/C_{ox}.$$

The gate voltage directly controls the charge in the semiconductor as described in the standard MOSFET theory (Equation 2.1). In a standard MOSFET the oxide thickness d is much larger than the inversion layer width W_{inv}. In the case of $C_{ox} \gg C_s$ Equation 2.9 simplifies to $V_g = \Psi_s + \text{const}$. The gate voltage directly controls the surface potential Ψ_s of the semiconductor [7]. The ratio of these two capacitances has to be studied when scaling the oxide or the bulk silicon down.

In a semiconductor any local charge is screened within the so-called Debye screening length $L_D = \sqrt{kT\varepsilon_0\varepsilon_{Si}/ne^2}$ which is in the range of $L_D = 40\,\text{nm}$ for $n = 10^{16}\,\text{cm}^{-3}$ [1]. If the wire is smaller than the Debye screening length L_D, surface charges cannot be screened. For thin wires the carrier density n gets more and more uniform within the wire cross-section. The same holds for the Fermi energy within the wire which is now equal to the surface potential $E_f = e\Psi_s$. In this case the carrier density in the semiconductor is described by the density of states (DOS). The semiconductor capacitance in this special case is called quantum capacitance C_q and $C'_q = C_q/A$ is

$$C'_q = e\frac{dn}{d\Psi_s} = e\frac{dn}{dE_f/e} = e^2 \cdot DOS(E = E_f). \tag{2.10}$$

In the subthreshold regime the Fermi energy is in the band gap and therefore the DOS is zero. The subthreshold swing S given in Equation 2.7 is reduced and ideally reaches its limit [8, 9, 10]

$$S = \ln(10)\frac{kT}{e}\left(1 + \frac{C'_q}{C'_{ox}}\right) \approx \ln(10)\frac{kT}{e} = 60\,\text{mV/dec}, \quad T = 300\,\text{K}. \tag{2.11}$$

2.3 Carbon Nanotube FETs

2.3.1 Introduction to Carbon Nanotubes

Since carbon nanotubes (CNTs) were discovered by Iijima in 1991 [11] they made their way in many different fields of research and applica-

tions. The reason is their various fascinating properties. With a typical diameter of 1-20 nm they can reach a length of millimeters [12]. Being all of carbon they are chemically inert and they are very strong. Their Young's modulus is estimated to be around 1 TPa [13], which is the highest ever reported. They can be metallic or semiconducting, depending on their atomic arrangement (see Appendix A). One can think of carbon nanotubes as a sheet of graphene rolled up (see Figure 2.5). There can be multiple shells cylindrically within each other as shown in the TEM image of Figure 2.5. Such nanotubes are called multi–walled carbon nanotubes (MWNTs). In the following context we are interested in single–walled carbon nanotubes (SWNTs) unless specifically mentioned. A more detailed introduction into carbon nanotubes and their electronic properties can be found in the Appendix A.

The fact that there are semiconducting carbon nanotubes brought quickly the idea of building field-effect transistors. This was realized by Tans et al. [14] in 1998. In the last few years much effort was put into understanding and improving such carbon nanotube field effect transistors (CNT FETs). Even logic circuits consisting of several CNT FETs have been realized [15, 16].

There are two different approaches that are often used to model CNT FETs: the model of MOSFET-like structures and the model of Schottky barrier transistors (SBFETs).

1. In a traditional Si MOSFET (see Section 2.1) source and drain regions are highly doped, whereas the channel is undoped or oppositely doped (see Figure 2.1). An insulating oxide layer separates the metal gate from the channel. By applying a gate potential, an inversion layer is formed. A bias between source and drain leads to a current flow. The resistance of the transistor is tuned by varying the number of induced carriers via the gate.

2. In Schottky barrier transistors the semiconducting channel is contacted by metal electrodes. At the contacts, Schottky barriers are present. The transistor operates by modulating the width of the tunnel barrier and, therefore, the current that flows from the contact.

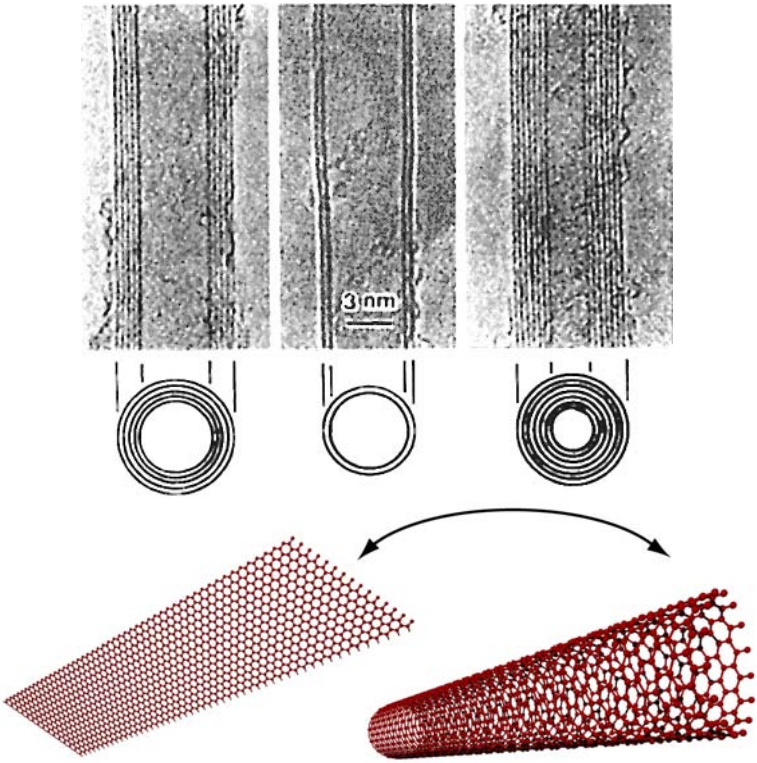


Figure 2.5: Top: TEM image of multi–walled carbon nanotubes, adopted from [11]. Bottom: Schematics of a sheet of graphene and a single walled carbon nanotube.

The first CNT FETs were described by charge modulation [14] in a MOSFET approach. The Schottky barrier model [17] was introduced explaining ambipolar behavior. The two models will be introduced next and compared in Section 2.3.4.

2.3.2 Carbon Nanotube MOSFET model

An applied gate voltage V_g will induce charge carriers in the nanotube that can contribute to a current passing the NT. Section 2.10 shows in general that depending on the semiconductor capacitance, the induced charge density might not linearly depend on the gate voltage. But the surface potential — which corresponds to the Fermi energy in case of nanotubes — can be related to the applied voltage. For this reason we are going to estimate the Fermi energy within the CNT when a gate voltage V_g is applied, then we will calculate the number of induced carriers from the Fermi energy and finally estimate the conductance G as function of the back–gate voltage V_g.

In analogy to the MOSFET theory where the MOS capacitance is studied, we first look at the silicon–oxide–CNT structure here (Figure 2.6 (a)). The capacitance $C = dQ/dV$ of this structure is best described by the model of a thin metallic wire at distance d from an infinitely large metallic plate [18]. If the radius of the wire r is much smaller than the distance to the metal plate $r \ll d$ a simple solution can be given for the capacitance per unit length $C^{\star}_{ox} = C_{ox}/L$:

$$C^{\star}_{ox} = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{2d}{r}+2\right)} \sim 20\,\mathrm{pF/m}. \tag{2.12}$$

The nanotube is not surrounded by one single gate dielectric. Between the gate and the nanotube there is SiO_2 with $\varepsilon_{SiO_2} \approx 3.9$, whereas above is air with $\varepsilon_{air} \approx 1$. This has to be taken into account by an effective dielectric constant $\varepsilon_r^{eff} \sim \varepsilon_{SiO_2}/2 \sim 2$ as shown in [18] and [19]. With an oxide spacing of $d = 400\,\mathrm{nm}$ and a tube radius of $r = 2\,\mathrm{nm}$ this leads to $C^{\star}_{ox} \sim 20\,\mathrm{pF/m}$.

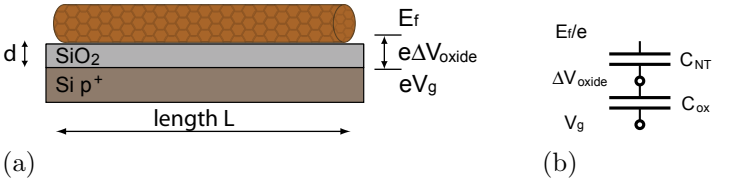


Figure 2.6: Silicon–oxide–CNT structure (a) with analogous circuit (b) consisting of oxide capacitance C_{ox} and quantum capacitance C_{NT}.

The CNT in a silicon–oxide–CNT structure cannot completely screen the electric field of the applied gate voltage as a metallic capacitor plate could. The potential within the CNT in not zero, but corresponds to the local Fermi energy E_f. The potential drop in the oxide is the difference between the applied voltage and the potential of the Fermi Energy within the CNT

$$V_g - \frac{E_f}{e} = \Delta V_{ox} = \frac{Q_{ind}}{C_{ox}}$$

where Q_{ind} is the total induced charge and $C_{ox} = C^{\star}_{ox} \cdot L$ is the oxide capacitance (Equation 2.12).

How does the Fermi Energy depend on the applied gate voltage? We take the derivative

$$\frac{dV_g}{dE_f} = \frac{1}{e} + \frac{1}{C_{ox}} \frac{dQ_{ind}}{dE_f} = \frac{1}{e}\left(1 + \frac{C_{NT}}{C_{ox}}\right) \tag{2.13}$$

with the quantum capacitance $C_{NT} = e \cdot dQ_{ind}/dE_f$. The quantum capacitance is given by the density of states (Equation 2.10) because with the one dimensional carrier density n, the total induced charge per unit energy is $dQ_{ind}/dE_f = eL \cdot dn/dE_f = eL \cdot \mathrm{DOS}$. With this, we can give an approximation for the quantum capacitance for energies well above the band edge. There the density of states is $\mathrm{DOS} = 8/(3\pi a_{CC}\gamma) = 2.0 \cdot 10^9\,(\mathrm{m} \cdot \mathrm{eV})^{-1}$ (see Appendix Equation A.15 for derivation) and the quantum capacitance per unit length is

$$C^{\star}_{NT} = \frac{C_{NT}}{L} = e^2 \cdot \mathrm{DOS} \simeq 320\,\mathrm{pF/m} \qquad \text{for} \quad E \gg E_c. \tag{2.14}$$

The fraction C_{NT}/C_{ox} depends strongly on the thickness of the gate oxide. For a rather thick oxide layer, as the 400 nm we often used, the oxide capacitance is smaller than the quantum capacitance. For a simple approximation we estimate the fraction by using the values of Equations 2.12 and 2.14 to be on the order of $\frac{C_{NT}}{C_{ox}} \approx 16$. Note that the fraction depends on the Fermi energy and can deviate from the assumed constant value. This has to be considered in the subthreshold regime.

With this, we write the Fermi energy of the CNT in the silicon-oxide-NT structure as a function of the applied gate voltage:

$$E_f = e\frac{1}{1+\frac{C_{NT}}{C_g}}(V_g - V_0) \tag{2.15}$$

where V_0 is an offset voltage. Note that this does not exactly correspond to the threshold voltage as used in the experimental chapters. It is an artificial offset for the calculations below, that corresponds to the gate voltage needed to bring the Fermi Energy to the center of the band gap choosing a constant capacitances throughout band and band gap. Carbon nanotube FETs show a p-type behavior. For this reason hole conduction is considered here.

Next we calculate how many free carriers are induced into the CNT channel when a gate voltage V_g is applied. We consider the condition where the source-drain bias applied across the NT is small: $eV_{sd} \ll \mathrm{k}_B\mathrm{T} \approx 25\,\mathrm{meV}$. In this case we assume the potential along the CNT to be uniform. The product of the Fermi distribution and the density of available states (DOS) yields in the number of carriers per energy in the CNT. For the total number of free carriers in the CNT as a function of the Fermi energy we have to integrate over this product:

$$n(E_f) = \int \mathrm{DOS} \cdot f(E_f) dE \tag{2.16}$$

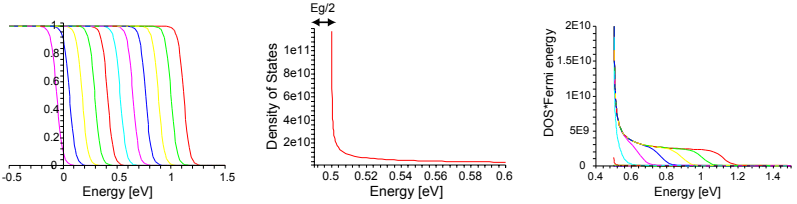
with the Fermi function (Figure 2.7 (a))

$$f = \frac{1}{1+\exp\frac{E-E_f}{kT}}$$

and the density of states of a semiconducting CNT (see Appendix Equation A.14)

$$\mathrm{DOS}(E) = \frac{8}{3\pi a_{CC}\gamma} \frac{|E|}{\sqrt{E^2 - (E_g/2)^2}} \Theta(|E| - E_g/2).$$

The DOS is plotted in Figure 2.7(b). Note that n is the number of charges per tube length as the 1D DOS is a density per length. The product $\mathrm{DOS} \cdot f(E_f)$ is plotted in Figure 2.7(c) for Fermi energy values belonging to different gating voltages as described in Equation 2.15.



(a) (b) (c)

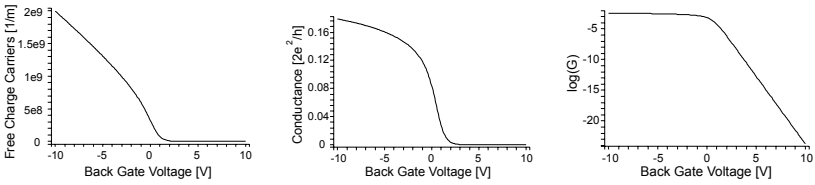
Figure 2.7: (a) Fermi distribution $f(E)$ for E_f given by Equation 2.15 at 300 K with $\frac{C_{NT}}{C_g} = 16$, $V_0 = 9\,\mathrm{V}$ and $V_g = -10, -8, ..., 10\,\mathrm{V}$.
(b) Density of States for a NT with $E_g = 1\,\mathrm{eV}$ (Equation A.14).
(c) The product $\mathrm{DOS} \cdot f(E_f)$ for the same gate voltages as in (a).

The integral 2.16 cannot be solved analytically. Results of numerical integration are shown in Figure 2.8 (a).

With the Drude model for diffusive transport we now can estimate the channel conductance:

$$G_{NT} = e\frac{n\mu}{L} \tag{2.17}$$

with the electron charge e, the length L of the CNT channel and the mobility μ. Here we assume the mobility to be constant. The total resistance of a device is characterized by the sum of the CNT channel resistance $R_{NT} = 1/G_{NT}$, the quantum resistance $\frac{h}{4e^2}$ and the contact resistance



(a) (b) (c)

Figure 2.8: (a) Number of free charge carriers (holes in this case), as function of applied gate voltage. (b) Conductance G and (c) $\log(G)$ of CNT FET as function of applied gate voltage calculated by MOSFET model Equations 2.16 and 2.18. Parameters: $V_0 = 9\,\mathrm{V}$, $\frac{C_{NT}}{C_g} = 16$, temperature 300 K, contact resistance $R_c = 50\,\mathrm{k}\Omega$, length of CNT channel $L = 1\,\mu\mathrm{m}$ and mobility $\mu = 2000\,\mathrm{cm}^2/\mathrm{Vs}$.

R_c. For this channel dominated model we assume the contact resistance to be constant. With this we obtain for the total conductance of the CNT FET

$$G = \frac{1}{\frac{h}{4e^2} + R_c + \frac{L}{e\mu n}}. \tag{2.18}$$

The conductance G as a function of the applied gate voltage is plotted in Figure 2.8 (b) as calculated by Equation 2.18 using numerical integration for the number of carriers n.

Let's have a look at two regimes of Equation 2.18: the linear regime and the subthreshold regime where the Fermi energy is just below the band edge.

Linear G vs. V_g regime

For high V_g the conductance is strongly suppressed. For high negative V_g the conductance saturates, limited by R_c and $h/4e^2$. In the linear regime of G vs. V_g in between, the total conductance is dominated by the channel

conductance given by Equation 2.17. From this we can calculate the slope as

$$\frac{dG}{dV_g} = \frac{e\mu}{L}\frac{dn}{dE_f}\frac{dE_f}{dV_g}.$$

The last term is given by Equation 2.13 and dn/dE_f can be derived from the integral 2.16. For energies well above the band edge we approach the Fermi function by a step function cutting off at E_f and then the derivative is $dn/dE_f = \mathrm{DOS}(E_f)$. Inserting this together with Equation 2.13 we arrive at

$$\frac{dG}{dV_g} = \frac{e^2\mu}{L}\mathrm{DOS}\left(1 + \frac{C_{NT}}{C_{ox}}\right)^{-1}.$$

With $e^2 \cdot \mathrm{DOS} = C_{NT}$ from Equation 2.14 we get

$$\frac{dG}{dV_g} = \frac{\mu}{L}\frac{C_{ox} \cdot C_{NT}}{C_{ox} + C_{NT}} \sim \mu\frac{C_{ox}}{L} \qquad \text{for} \quad C_{ox} \ll C_{NT}. \tag{2.19}$$

In the linear region of G vs. V_g the slope of $G(V_g)$ can be directly related to the carrier mobility μ and the geometry of the device expressed in L and C_{ox}. In Section 4.2.3 this relation is used to determine the mobility of our CNT FETs.

Subthreshold regime

In the second case of the Fermi energy being below the band edge, only thermally exited charge carriers can contribute to a current. The number of carriers is determined by the Boltzmann factor $e^{-(E_g/2-E_f)/(kT)}$. Neither contact and quantum resistances nor the density of states are limiting. The conductance is given by $G = e\mu/Ln_0e^{-(E_g/2-E_f)/(kT)}$. If we take the derivative of the logarithm $d(\ln(G))/dV_g$ we get

$$\frac{d(\ln(G))}{dV_g} = \frac{d(\ln(G))}{dE_f} \cdot \frac{dE_f}{dV_g} = \frac{1}{kT}\frac{dE_f}{dV_g}$$

In Section 2.1.4, the subthreshold swing S is defined as the gate voltage needed to suppress the current by one order of magnitude $S =$

$dV_g/d(\log(I))$. In the experimental part we generally plot the conductance at small bias voltage. So we have to transfer the above definition of S into conductance. Because the bias voltage is constant the conductance $G = I/V_{sd}$ scales in the same way and we can say

$$S = \frac{dV_g}{d(\log(G))} = \ln 10 \frac{kT}{e} \frac{1}{\alpha}. \tag{2.20}$$

The efficiency parameter $\alpha = e(dE_f/dV_g)$. In the subthreshold region α is constant. In the ideal case the Fermi energy follows the applied gate voltage and $\alpha = 1$. Then the subthreshold swing is $S \simeq 60\,\mathrm{mV/dec}$ at room temperature. In Figure 2.8(c) the logarithm of the conductance G is plotted against the back–gate voltage. In our simulation we find $S \simeq 400\,\mathrm{mV/dec}$. Note that a fixed $\alpha = C_g/C_{NT} = 1/16$ was assumed. In reality C_{NT} is expected to vanish in the subthreshold regime (see Section 2.2). For a device that is completely dominated by the channel resistance the subthreshold swing S could reach its ideal limit.

2.3.3 CNT Schottky Barrier Transistor model

The modelling of carbon nanotube Schottky barrier transistors is more difficult than that for MOSFET devices and numerical simulation [20] is essential. Therefore a qualitative description will be presented.

First we look at a mid-gap Schottky barrier structure. This means that the barriers to the conduction and valence bands are equal, as sketched in Figure 2.9 for the case of $V_d = 0$ and $I = 0$. For $V_g > 0$ the conduction band is pushed down and electrons tunnel into the conduction band from both contacts. For $V_g < 0$ the valence band barrier is thinned and the hole tunnelling is increased. Note that the bands are bent towards the contacts and flat in the central region.

Consider now the case where a bias V_d is applied and $V_g = V_{sd}/2$. In this case the band diagram is symmetrical from left to right as sketched in Figure 2.10(a). At the left, $V_g = V_{sd}/2$ and the left contact acts as a source of electrons. At the right contact, $V_g = -V_{sd}/2$ and the right contact acts as source of holes. Holes and electrons flow in opposite directions, so

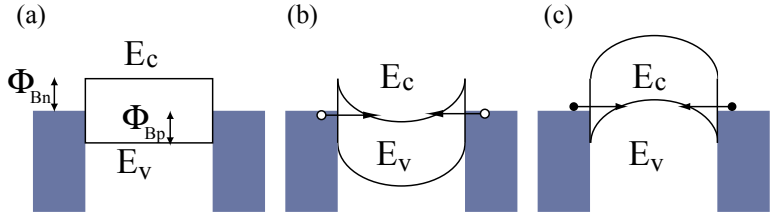


Figure 2.9: Schematics of CNT with metal contacts and Schottky barriers. Gate Voltage (a) $V_g = 0$, (b) $V_g > 0$ and (c) $V_g < 0$, ∘ indicate electrons in the metal tunnelling into the CNT, • indicate holes above Fermi energy of the metal.

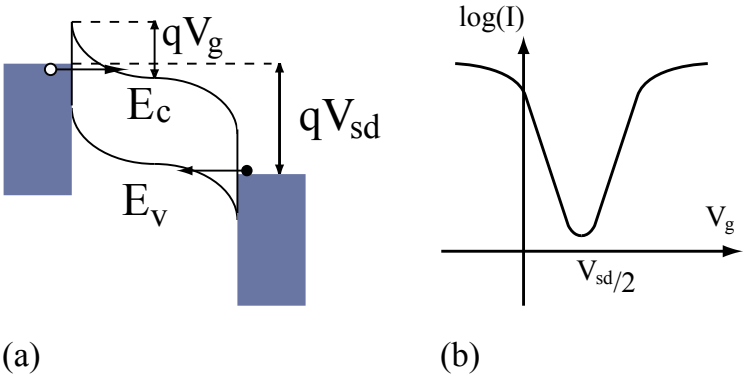


Figure 2.10: (a) Schematics of CNT with metal contacts and Schottky barriers at $V_g = V_{sd}/2$. (b) Sketch of ambipolar current vs. V_g at fixed V_{sd}. ∘: electrons in the metal tunnelling into the CNT, •: holes above Fermi energy of the metal.

the currents add. This is the minimum current of the Schottky barrier transistor. For $V_g > V_{sd}/2$, electron injection is enhanced and the device operates as an n-channel FET. For $V_g < V_{sd}/2$ it operates as p-channel FET. The behavior sketched in Figure 2.10(b) of enhanced current for both, positive and negative gate potentials is called ambipolar behavior [21].

A symmetric ambipolar behavior can only be observed if the barriers between metal and CNT have the same height for holes and electrons. In CNT FET the most widely used contact metals Ti, Au and Pd have high barriers to the conduction band, but low barriers to the valence band. Therefore hole conduction is favored.

In this model the behavior of a CNT FET in the subthreshold region is by tunnelling through the Schottky barrier. As this barrier is modulated by the gate, the current through the nanotube in subthreshold region depends on the coupling of the gate to the barrier. This coupling is controlled by the gate capacitance $C^{\star}_{ox}$. The thicker the gate oxide is, the more the subthreshold swing S deviates from its ideal value of 60 mV/dec (2.20) for a Schottky barrier dominated FET [22, 23]. For 120 nm SiO_2 a subthreshold swing of $S \sim 2000\,\mathrm{mV/dec}$ was measured [17] (see Section 4.2.3 for more experimental details). This is a big disadvantage of Schottky barrier dominated CNT FETs compared to low contact CNT FETs.

2.3.4 Experimental observations: Literature review

In literature both, channel dominated [24, 25] and Schottky barrier dominated devices [17] have been reported, and in many cases both effects might play a role [26, 27, 28]. Details of device geometry influence the effectiveness of the gate in modulating the carrier concentration in the channel [24] and in modulating the Schottky barriers [29, 17, 20]. Nanotube diameter and metal - nanotube contact critically determine the Schottky barrier height [30]. The role of the metal work function has been studied by different groups [25, 31, 30]. Pd makes very good contact for hole conduction [25, 32]. This is due to its good wetting properties

and its high work function (5.1 eV) which aligns the Fermi energy quite well with the CNT valence band. For Ti the Fermi energy lies deeper in the nanotube band gap, so that injection of both, holes and electrons is possible leading to ambipolar FETs. Quite good contact can be achieved by annealing [21]. Al has a low work function (4.1 eV) and the barrier to the conduction band is much smaller. Therefore electron transport is favored [31]. We designed our CNT FETs to have low contact barriers for holes as described in Section 3.2.

In summary the basic physics of MOSFET devices is described in Section 2.1 of this chapter. When scaling the devices down to nanowire like structures, the ratio C_s/C_{ox} has to be studied. In depletion C_s is given by the depletion capacitance C_d for bulk MOSFETs and deviates for nanowires of diameter $d < W_d$. For small nanowires $d \ll L_D$ and for carbon nanotubes C_s is given by the quantum capacitance C_q. For CNT FETs a simple model is developed based on the standard MOSFET theory. It shows the basic physics. Assuming realistic values for μ and R_c of high quality CNT FETs the quantitative outcome is in good agreement with observations described in Chapter 4.

CHAPTER 3

Sensor fabrication techniques

Silicon nanowire (SiNW) FETs and Carbon Nanotube (CNT) FETs were produced by different approaches: For SiNW FETs the structure was designed by lithography and transferred into the device layer of a Silicon on Insulator (SOI) wafer. CNT FETs were produced by localizing and contacting randomly grown carbon nanotubes (CNTs). Whereas the fabrication scheme for SiNW FETs is fully CMOS compatible, the approach used for CNTs can be used for research purpose only, as chemical vapor deposition of CNTs is not CMOS compatible and the fabrication scheme is sequential and very time consuming. Both processes are described below. Experimental details about the developement of processes can be found in Appendix C.

3.1 Silicon NW FET

Silicon Nanowire FETs (SiNW FET) were produced by etching the structure into the device layer of a SOI wafer. The silicon substrate — called handle layer — is used to apply a gate voltage and is therefore called back–gate.

As starting material a SOI wafer with 150 nm buried oxide (BOX) and a 100 nm thick device layer was used. It was p-doped by boron with a resistivity of $10 - 20\,\Omega$cm and was purchased from CSD Silicon. The fabrication of SiNW FETs is shematically shown in Figure 3.1. In short it contains the following steps:

1. Thermal oxidation of a 80 nm thick top silicon oxide layer. By this step the device layer is thinned to ~ 60 nm.
2. Defining the etch mask of chromium:
   - Structure of contact pads and connection leads defined by photolithography and deposition of 80 nm Cr.
   - Structure of nanowires and small leads defined by e-beam lithography and deposition of 100 nm Cr.
3. Etching of the structure:
   - Plasma etching of the top SiO_2 using the Cr layer as etch mask. Plasma etching consists of a cleaning step of oxygen plasma, an unselective SiO_2 etching by a mixture of CHF_3 and oxygen plasma and a selective etching by CHF_3 that stops on the Si device layer.
   - The chromium mask is removed by wet etching with a mixture of NaOH, $KMnO_4$ and H_2O (with a ratio 2:3:12) under constant shaking.
   - The device layer is etched by Tetramethylammoniumhydroxide TMAH (25%) and 10% isopropanol in H_2O at 45° C under constant stirring. A buffered HF dip just before this TMAH bath is needed to remove the native oxide.

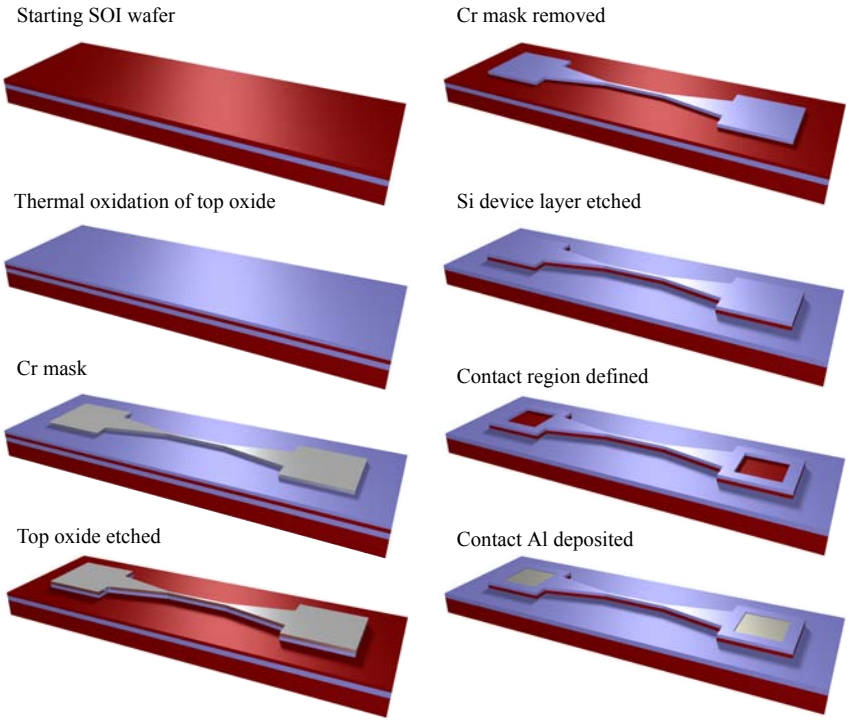


Figure 3.1: Schematics showing the fabrication steps of Si NW FETs. The red color stands for Si, the blue one for SiO_2.

4. Contacts are created by a photolithography step to define the contact region, a buffered HF etching step to remove the top SiO_2 in the contact region, in situ Ar sputtering and deposition of 100 nm Al. The contacts have to be annealed at 450°C for 10 to 30 minutes to get ohmic contacts.

3.1.1 Top oxide

The top oxide is used as etching mask for the TMAH etching step and as protecting layer for the leads working in liquid environment. Thermal oxidation was performed at the PSI. The top oxide thickness is $70-80$ nm. One can estimate the consumed Si to be $0.46 \cdot x_{ox}$ [33]. This gives $33-37$ nm of consumed Si and thus the remaining device layer is expected to be $62-68$ nm thick. It is known that during the thermal oxidation of SOI wafers, some oxygen can diffuse through the device layer and lead to an increase of the buried oxide so that the device layer shrinks more than expected from conventional silicon wafer oxidation [34]. But this effect should be < 5 nm. The device layer thickness after oxidation is 60 nm, as measured by an Alpha-Step surface profiler.

3.1.2 Etching mask

The structure of the mask can be seen in Figure 3.2. Contact pads are designed in a decent distance from the active region because for the use in sensing experiments, they have to be insulated from liquid. Contact pads, leads and alignment marks are designed by photo lithography. Nanowires are designed by e-beam lithography. The shape of the nanowire mask could be varied. Typical length is $1-10\,\mu$m and the width is ~ 80 nm.

Chromium was chosen as etch mask because it can easily be evaporated and removed selectively to Si and SiO_2 by a simple wet etching step and it can easily be seen in the SEM. Organic masks like photo resist or e-beam resist lead to problems as they can hardly be removed after CHF_3 plasma etching. The thickness of the Cr film is chosen to be as thin as possible to minimize the aspect ratio of the mask of the nanowires. Limiting factor

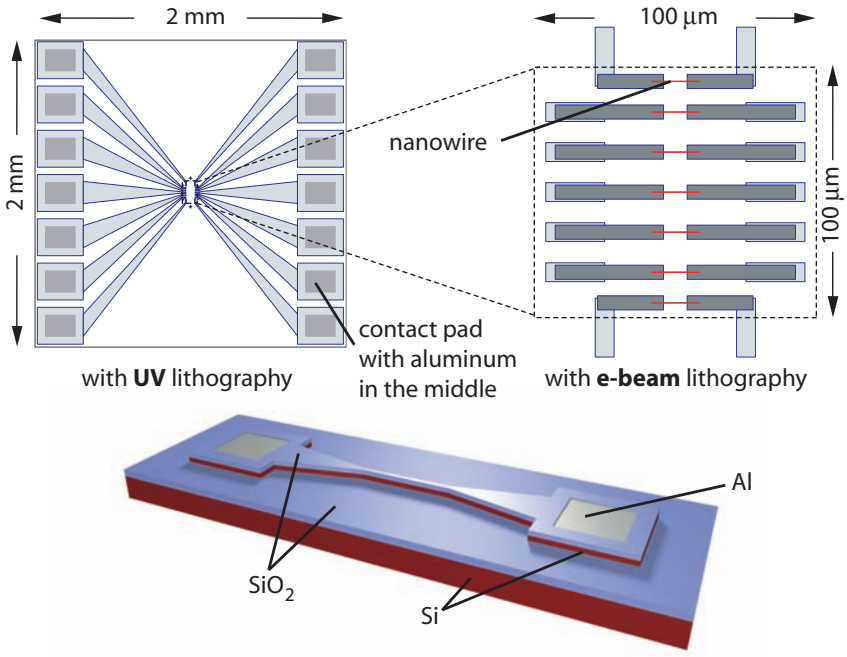


Figure 3.2: Structure of mask for SiNW fabrication.

was the fact that the same Cr layer has to be used for alignment for the subsequent e-beam lithography step - and therefore the Cr mask has to be visible in the SEM even below the resist layer. The first evaporated Cr layer is chosen to be 80 nm. The second Cr layer is 100 nm and it is evaporated in three steps: 20 nm perpendicular and then twice 40 nm tilted by an angle of $\pm 12^\circ - 15^\circ$ towards the two contacts to ensure good overlap with the first Cr layer (see Figure 3.3).

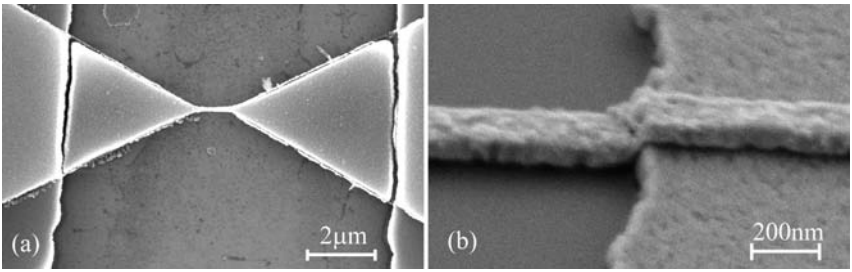


Figure 3.3: Overlay layer at metal evaporation. (a) Cr layer of 100 nm evaporated perpendicular on a Cr layer of 60 nm. It can be seen that the upper layer is not connected. (b) nicely connected 60 nm Au layer on top the same bottom Cr layer.

3.1.3 Etching of the device structure

In a first step, the top SiO_2 is etched using the Cr structure as etching mask. Before the the sample is cleaned by an oxygen plasma step of two minutes at a power of 200 W. Then the SiO_2 is etched by a CHF_3 plasma (40 sccm (standard cubic centimeters per minute) at 25 mTorr, 100 W power) with addition of 2 sccm of oxygen for 90 s and for another 2 min without oxygen. The oxygen is added since it was found that it makes the etched surface smoother. This can be seen by an AFM analysis shown in Figure 3.4. But when adding oxygen, the plasma etch does not stop at the Si layer any more, as one can see from the etching rates in Table 3.1. Therefore the last few nanometers of SiO_2 are etched down to

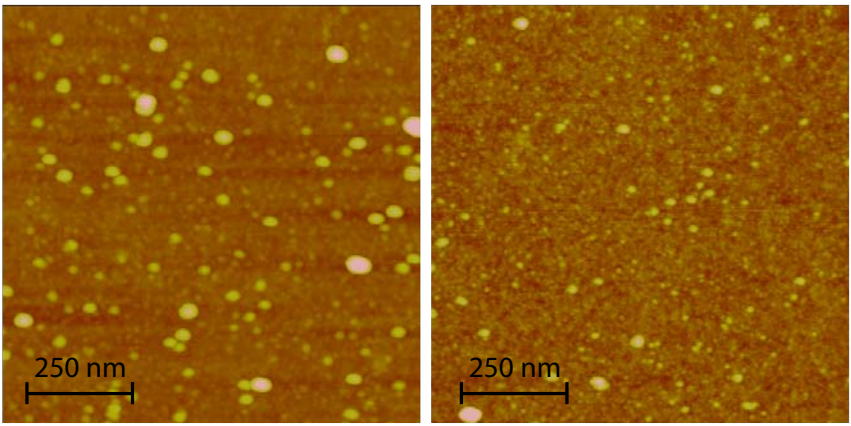


Figure 3.4: AFM images of Si surface with top SiO_2 etched away. Left: the result of a CHF_3 plasma (40 sccm/min) process is shown. Right: the result of a mixed CHF_3 (40 sccm/min) and oxygen (2 sccm/min) plasma is shown.

the Si without addition of oxygen.

Table 3.1: Etch rates of CHF_3 plasma etch processes.

	SiO_2	Si	PMMA
CHF_3	21 nm/min	$\sim$ 2.5 nm/min	$\sim$ 10 nm/min
CHF_3 + O_2	21 nm/min	$\sim$ 8 nm/min	$\sim$ 30 nm/min

When the top SiO_2 is etched, the Cr mask can be removed by a wet etching step. A mixture of NaOH, $KMnO_4$ and H_2O (with ratio 2:3:12) is chosen because it does not attack Si or SiO_2 and because it etches both, chromium and chromium oxide [35]. It etches Cr with a rate of ~ 30 nm/min, after an initialization time of $60 - 90$ s. But to ensure that no Cr clusters are left, one has to etch several minutes in addition and strong stirring or shaking is needed. To avoid left overs sticking on the

surface, the first washing step after etching was done under shaking as well.

Before etching the device layer, the native oxide on the silicon has to be removed by a 20 s dip in buffered HF. A mixture of 21 ml HF (40%) + 148 ml H_2O + 155 g NH_4F was chosen for an etch rate of 40 nm/min.

Tetramethylammoniumhydroxide (TMAH) was chosen for etching the Si device layer because it is very selective to SiO_2 and etches anisotropically [36, 33]. It is very well suited for etching nanowire like structures [37]. With an etching rate of ~ 70 nm/min in Si $\langle 100 \rangle$ direction, a short etching time is enough to etch down the device layer. But an etching time of 15 min was used to ensure that TMAH etches to Si $\{111\}$ surfaces. These are etched much slower and should build nice side walls of our nanowires (see Appendix C.1).

The etch rate depends very much on temperature so that it has to be controlled well. Therefore the etchant was stabilized in a temperature bath at 45° C. 10% 2-propanol was added to the TMAH solution (25% in H_2O) to reach smoother etching. Constant stirring is important to reach homogenous etching results. More details about TMAH etching are described in Appendix C.1.

TMAH etches Si $\{111\}$ planes much slower then other planes. On silicon (100) wafers the nanowires have to be oriented in a $\langle 110 \rangle$ direction (see Appendix C.1) to ensure that the nanowire sidewalls are $\{111\}$ planes. In this case the sidewall is not perpendicular to the top surface, but under an angle of 54.47°. This leads to a trapezoid like shape of the wire as shown in Figure 3.5. Typical dimensions are 60 nm for the height h and 40 nm to 120 nm for the width of the SiO_2 mask. The top width of the nanowire is expected to be thinner due to underetching of the mask. Because of the trapezoid shape the bottom width is ~ 80 nm wider than the upper part (see Figure 3.5(c)). The nanowire width was estimated by SEM and AFM as the examples of Figure 3.6 show. In case of thin masks or short TMAH etching one can clearly see that the bottom of the NW is wider than the mask. For longer etching times the undercut is too big so that the bottom width cannot be resolved. We estimate the mean width of the NWs to be in the range of $W \sim 100$ nm typically.

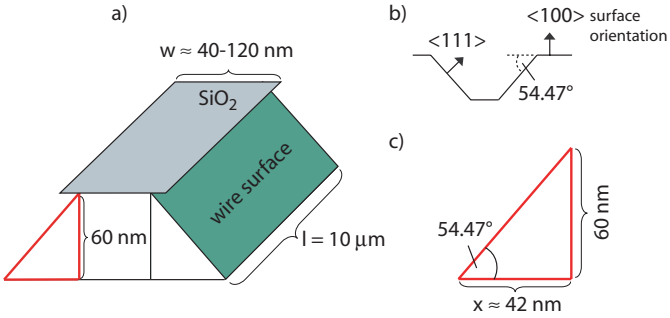


Figure 3.5: Sketch of geometric dimensions. (a) Height $h = 60\,\text{nm}$, grey: SiO_2 mask, green: non vertical SiNW side wall. Geometrical proportion for anisotropic etching is shown in (b). The additional width at the bottom is geometrically well defined (c).

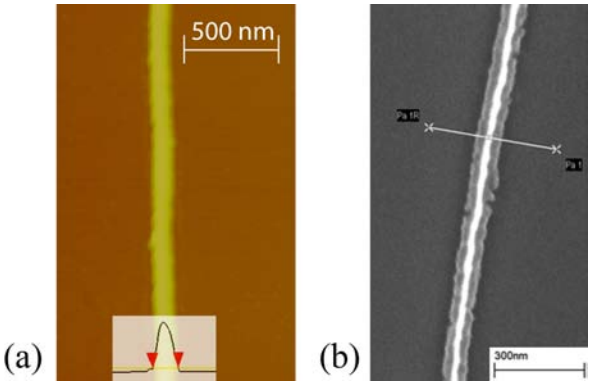


Figure 3.6: Images of two silicon nanowires. (a) From AFM one can estimate the bottom width of 136 nm for wire (a). (b) From SEM image the top width can be estimated to $\sim 20\,\text{nm}$ for wire (b).

3.1.4 Contacts

The contact region is defined by photo-lithography. The SiO_2 is etched by buffered HF. This is better suited than plasma etching since it attacks the underlying Si less and when using CHF_3 plasma in combination with photo resist, the resist is hardened so that it cannot be dissolved after the etching step. To prevent HF to flow between the sample and the photo resist, an adhesion layer of hexamethyldisilazane (HDMS) is spun on the sample just before the photo resist. After photo lithography the HDMS is ashed in the open parts by 3 min UV - ozone. This helps to remove leftover photo resist which is important for homogeneous etching.

The samples were built into the vacuum chamber of the evaporator just after removing the SiO_2 to avoid oxidation of the Si. In addition the sample is sputtered with Ar plasma for 20 s short before evaporation of Al to remove any eventually new oxide in the contact region and to roughen the Si surface. 100 nm of Al is evaporated at low pressure ($\sim 1 \cdot 10^{-7}$ mbar) with high rate to avoid oxygen to react with the Al.

After lift-off, the contacts are annealed at 450° C for $10-30$ min in forming gas (mixture of Ar and H_2) to form ohmic contacts.

3.1.5 Summary SiNW FET devices

Most SiNW FET sensors reported in literature are fabricated by a "bottom–up" approach of positioning and contacting grown SiNWs [38, 39] or in place growth [40]. In all these devices as well as in recently reported "top–down" fabricated structures [41, 42], the metal contact or heavily doped Si is in direct contact with the SiNW. This way the contact region is dominated by two effects: the geometrical confinement and the material junction. Here these two effects are separated by introducing semiconducting leads. A "top–down" approach to fabricate SiNW FETs has been developed with the following features designed for sensing experiments:

- Semiconducting leads ensure that there is no p-n or metal–semiconductor junction at the edge of the wire.

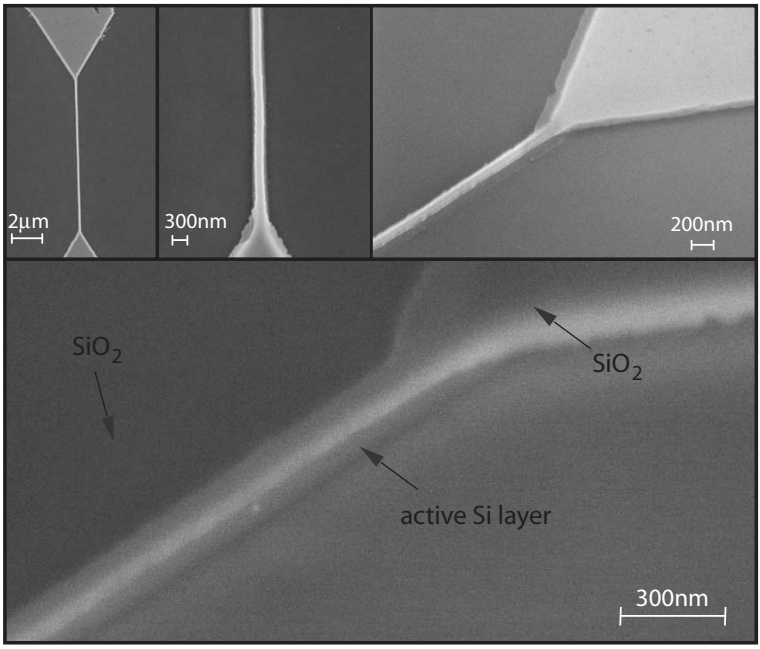


Figure 3.7: SEM picture of SiNW FETs with $L = 10\,\mu$m in top view (small images top left) and in side view.

- The SiNW channel is directly exposed to the environment so that it can be used for sensing.
- Top oxide avoids leakage currents between the leads when working in an electrolyte.
- The gate is insulated from the liquid by the buried oxide.
- Clean sidewalls are produced by TMAH so that a high aspect ratio (length:width > 100) can be reached for NWs in the range of $W \sim 100\,\text{nm}$.
- Standard SOI wafers with thin BOX and device layer can be used.
- The design is flexible and allows combination with on-chip electronics or microfluidics.
- The width of the SiNWs can be adjusted by controllable under etching of the SiO_2 mask in the TMAH wet etch process. This is important for application in the field of sensing. As we will show in Section 5.1.2, the sensitivity of the SiNW response to a change in surface potential can be tuned by adjusting the wire width. Controlling the width by etching would allow combining SiNW FETs of varying sensitivity to enhance the dynamic range.

Figure 3.7 shows SiNW FETs with $L = 10\,\mu\text{m}$. The top SiO_2 can bee seen in all pictures, the Si sidewall can be recognized in the two pictures of viewing under a tilt angle.

3.2 Carbon Nanotube FET

The fabrication of SWNT Field Effect Transistors is illustrated in Figure 3.8. SWNTs were grown by Chemical Vapor Deposition (CVD) on Si wafers with 400 nm thermally grown SiO_2. Then alignment markers and bonding pads of SiO_2/Ti/ Au were prepared. SWNTs were selected and located by SEM. Then the SWNTs were contacted by Pd or Ti / Au. For

the passivation of the contacts different schemes were used as described in Section 5.6.1. The first subsection gives a general overview of fabrication issues of carbon nanotube FETs (CNT FETs) to justify the chosen approach. More details about our fabrication scheme can be found in the following Subsections (3.2.2-3.2.4), alternative fabrication approaches are described in Appendix C.3.

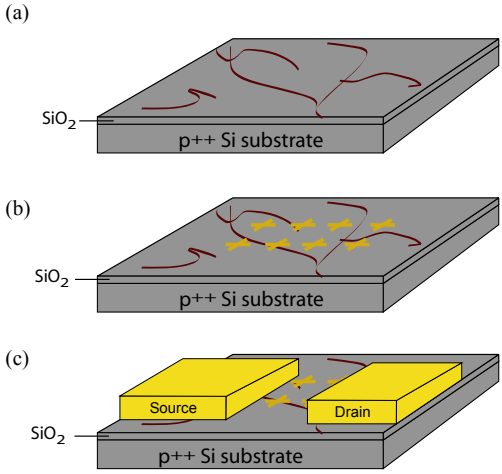


Figure 3.8: Fabrication Scheme for CNT FETs: (a) CNT growth, (b) patterning of markers, (c) deposition of metal contacts

3.2.1 General device fabrication issues

Today's processes for device fabrication of CNT FETs of individual SWNTs are far away of being efficient and reliable. Many different approaches for efficient and controllable device fabrication are under investigation. One issue is how to place and align CNTs where they are needed, another issue is how to get a specific type of CNTs. A third issue is the compatibility of CNT device fabrication with CMOS technology. All these issues

have to be addressed for the two possible main routes of growing CNTs directly on the substrate and of deposing CNTs from solution.

Positioning of CNTs

In CVD growth of CNTs their position can be chosen by selective positioning of catalyst. Many different approaches have been examined. Among them are: Conventional lithography and lift-off technique for rather big catalyst islands [32], micro contact printing [43] and self assembly of iron containing macromolecules [44].

Orientation of CNTs during CVD growth was achieved by gas flow [45], by an electric field or by growth along crystaline steps of the substrate [46]. I regularly observed orientation of nanotubes with laminar gas flow, but only for very long tubes ($\geq 100\,\mu$m).

Selective positioning of nanotubes from solution was achieved by dielectrofloresis [47], by tuning the hydrophobicity of metal and substrate with self assembled molecular monolayers [48, 49, 50] or by molecular recognition of modified CNTs with modified contacts [51, 52].

As all these techniques are not yet fully developed, we design the contacts to fit to randomly grown tubes. This is a time consuming process but allows to control that only a single tube bridges the contacts.

Selection of CNT Type

In CVD of SWMNTs the diameter can be controlled by the size of the catalyst particles and by the chosen temperature [53, 54, 55]. In this way the diameter distribution can be tuned well. But to narrow down the distribution is a task which is still under hard investigation [53]. To narrow down the distribution to the level of chirality selectivity, other parameters have to come into play that help stabilizing the growth like co-catalysts or stabilizing effects of the substrate [56].

Solving SWNTs in water with single-stranded DNA oligomers as surfactant is diameter dependant. Using different DNA sequences SWNTs of

different diameter could be separated [57]. Metallic or semiconducting CNTs could be deposited with high selectivity by dielectrophoresis [47]. A very critical issue in deposing SWNTs from liquid is to avoid bundeling. A lot of studies can be found about solvents, surfactants and deposition methods [58, 59, 60].

Some effort in fabrication of CNT FETs with tubes from solution is discussed in Appendix C.3. Finally we decided to grow tubes by CVD as described in Section 3.2.2.

CMOS technique compatibility

For CVD growth of SWNTs directly on chip the high temperatures required for the decomposition of the gases is destructive for any CMOS based chip. Efforts are put in bringing down the required temperature of CVD by choice of catalyst and by plasma enhanced CVD. Such principle based incompatibilities can be avoided in liquid based deposition of nanotubes. But in the process of separation and selective positioning of CNTs from liquid, chemicals are needed that are far from being desired in any CMOS compatible clean room. For our research purpose none of these restrictions are relevant.

CVD growth on substrate and deposition of CNTs were both tested (see Appendix C.3) but finally we stick to CVD growth as described in the next Section.

3.2.2 Chemical Vapor Deposition

Different techniques can be used to produce Carbon Nanotubes: Arc-discharge, laser ablation, High Pressure Carbon dioxide growth and catalytic Chemical Vapor Deposition (CVD) of hydrocarbons. The last method was chosen because CNTs can be grown on the substrate directly. All other production methods give a CNT powder that has to be purified, suspended in solvents and then deposited on a suitable substrate. There remain many problems in a solution-based device fabrication

process. First, the nanotubes have to be purified. This normally involves strong acid treatment and sonication, which may introduce defects into the nanotubes and cut them into short pieces. Secondly, nanotubes tend to bundle and surfactants are used to separate them efficiently, but surfactants are not desired for contacting the nanotubes.

By CVD, carbon nanotubes can be grown horizontally on the substrate and are clean enough so that they can be contacted without any purification step, which greatly reduces the possibility of defect formation of SWNTs. Measurements in our group and others have shown that devices made of CVD nanotubes grown directly on substrates tend to exhibit better performance than those produced using SWNTs prepared by other methods [61]. One of the reasons is the large diameter that CVD tubes typically have [30], another reason is that surfactants used in the deposition can lead to an additional contact resistance.

The CVD process is based on the method developed in the group of H. Dai [62]. The substrate covered with a catalyst of $FeNO_3$, $MoCl_2O_2$ and AlO_2 (preparation recipe in Appendix C.2) is heated in a furnace to 900° C – 1000° C under Ar flow. Hydrogen and the feeding gas (methane) are flown during 10 min for CNT growth.

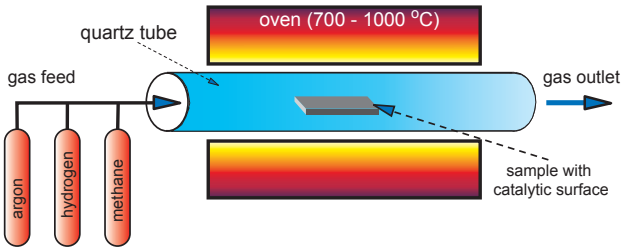


Figure 3.9: Scheme of CVD setup used for growth of carbon nanotubes.

The CVD furnace is sketched in Figure 3.9. Catalyst is spun on a freshly cleaned wafer. The samples are introduced into the quartz tube on a small boat. The gases are fed into the system by a pressure of 0.1 bar above

atmospheric pressure. A water bubbler at the outlet gives us control over the flow and avoids environmental gases to diffuse into the system.

Argon runs during heating up and cooling down (800 sccm/min). Different growth temperatures were used, but best results were achieved with a temperature of 950° C. During growth, argon was switched off. Methane (1300 sccm/min) and hydrogen were flown for 10 min. After growth methane is replaced by argon, but hydrogen still runs while cooling down to 550° C. From this temperature down to about 200° C only argon flows.

The temperature during growth has to be high enough to ensure that there are only SWNTs, not double-walled or multi-walled. But if temperature is too high, amorphous carbon is deposited. Hydrogen reduces the deposition of amorphous carbon, but it competes with the growth process [63]. Therefore the flow of hydrogen was chosen moderately. For more details see Appendix C.2.

3.2.3 Selection and location

Scanning Electron Microscopy (SEM) was used to select and locate SWCNTs. A typical acceleration Voltage of 1 kV was used to image SWNTs on silicon wafers with SiO2. At such low acceleration voltage the used SEM (LEO Supra 35) has a resolution limit of about ten of nanometers. Still individual carbon nanotubes can be seen. To check that we see all the SWNT in SEM, a comparison between a SEM and AFM image of the same sample is shown in Figure 3.10.

The advantage of the AFM is its much higher resolution that the SEM. To prevent damaging the tubes tapping mode AFM was chosen. The SEM is however much quicker and easier to be used than the AFM. One can be relatively sure that every tube can be seen in an AFM scan of the surface but it was not obvious if they would appear on SEM pictures due to lower resolution of the SEM. By scanning the same area using AFM and SEM and comparing the results it was estimated if everything could be also seen in the SEM images.

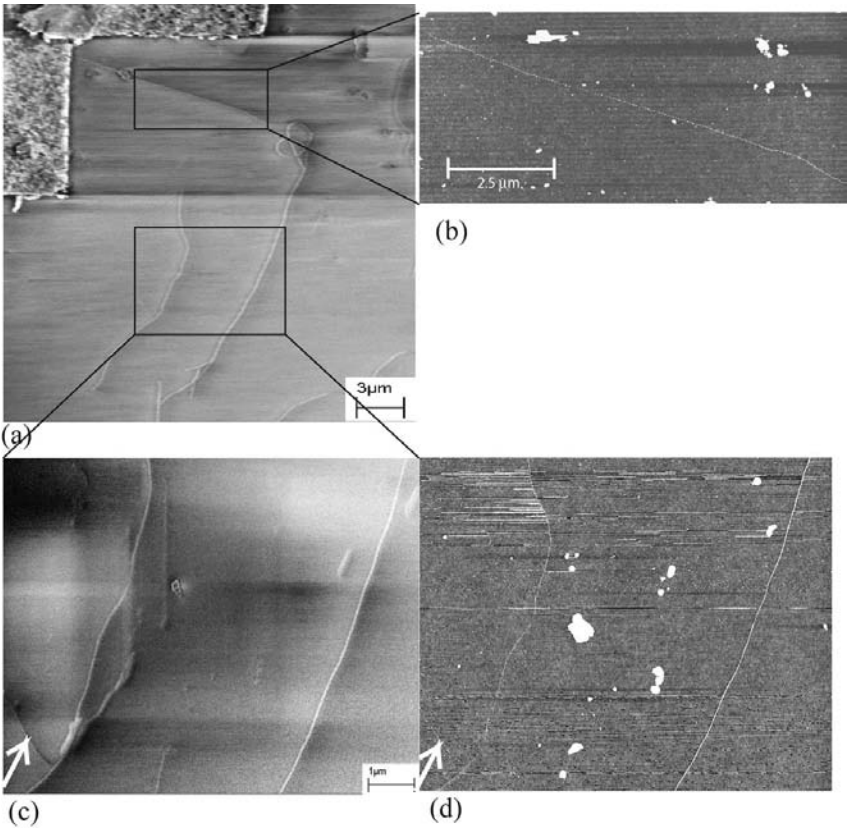


Figure 3.10: SEM (a) and (c) and AFM (b) and (d) pictures of the same region. In SEM the CNTs can be seen even at quite low magnification due to their high contrast to the background. The AFM has a much higher resolution and the background is imaged much more detailed. It even makes it hard to see the tubes. The very small tube indicated with an arrow in (c) and (d) is harder to find in the AFM picture (d) then in the SEM picture (c). (CNTs grown by methane at 950° C.)

Practically all tubes that are seen in AFM can also be seen in SEM. This is an important result. In SEM the CNTs can be seen even at quite low magnification due to their high contrast to the background. The high contrast comes from the different electronic properties of CNTs and the silicon oxide substrate. It depends very much on the acceleration voltage. At low voltage tubes seem bright when looking at backscattered electrons. The AFM has a much higher resolution and the background is imaged in much more detail. The surfactant or catalyst particles lying around are much bigger than the CNTs and therefore the feedback system of the AFM cannot be optimised to image the CNTs. This makes it even harder to see the small tubes. But we are pretty convinced that by careful imaging both, AFM and SEM can show all the tubes. According to this the SEM can be used to scan samples for nanotubes. One can localise the nanotubes for contacting and roughly estimate from the SEM pictures if the nanotubes are likely to be individual or not.

An open question is still how invasive the e-beam exposure is on CNTs. Strong influence of e-beam exposure of carbon nanotubes has been reported [64, 65], mainly for high voltages. But the good properties of the nanotube FETs produced this way show that short imaging does not strongly affect them. Even exposing contacted nanotubes to an e-beam dose of $500\,\mu\mathrm{As/cm^2}$ at 35 kV does not influence their conducting properties (See Section 5.6.1).

3.2.4 Contacting CNTs

Two steps of lithography and metal deposition were used. A typical structure of the first one is shown in Figure 3.11 in yellow. It shows the bonding pads, long leads to the inner part and small alignment markers and a side gate designed for electrolyte gating. On this structure 10 nm SiO_2, a 10 nm Ti adhesion layer and about 40 nm Au were deposited. Sometimes bundles of nanotubes with a length of several hundred micrometers made a short between the leads. The SiO_2 below the leads insulated the leads from these tubes and prevented from shortage problems.

In a second lithography step the contact leads were designed to contact

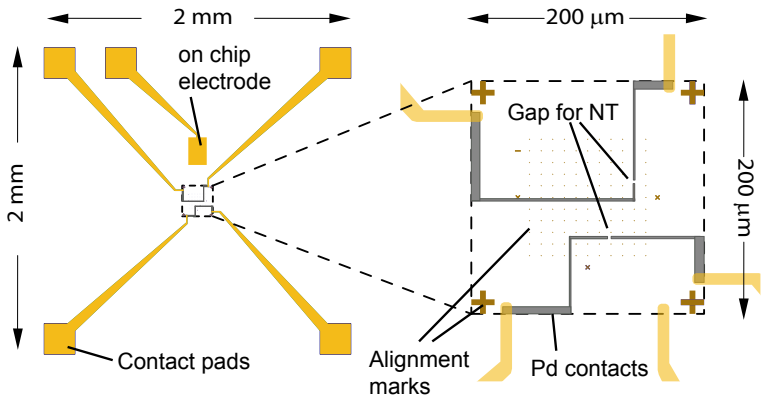


Figure 3.11: Mask for metal deposition for CNT FETs.

the selected nanotubes to the leads defined in the first step. The structure is shown in Figure 3.11 in grey. These contacts are made by Ti / Au or Pd. The latter is chosen mostly as it makes much better contacts due to its wetting properties and because the work function matches nicely the CNT band gap.

3.2.5 Summary CNT FET fabrication

As an optimal fabrication approach for CNT FETs for sensing purpose CVD was chosen for the following reasons:

- CVD tubes can be used as grown, no purification and no surfactant is needed that would alter the surface properties.
- Tubes grown on substrate bundle less than CNTs in powder and solution.
- CVD results in CNTs of rather high diameter of $\sim 1-3\,\mathrm{nm}$. This

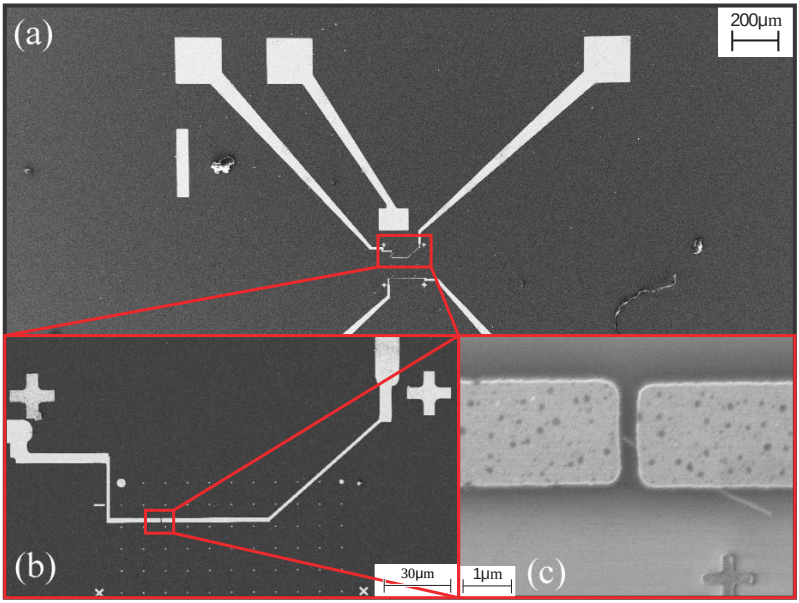


Figure 3.12: SEM images of a CNT FET. Overview (a) with zoom in (b) showing alignment marks and contacting leads. (c) is a zoom in of (b) showing the gap with the CNT bridging.

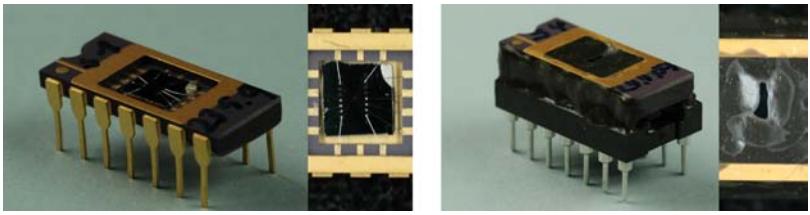
favors high contact transparency. Good conducting properties of CNTs from our CVD process are shown in the next chapter.

CNTs are localized by SEM before contacting so that we are sure that only one tube bridges the contacts. Palladium was chosen as contact metal for its good contact properties. SEM pictures of a CNT FET are shown in Figure 3.12.

3.3 Packaging

All devices were glued on a chip carrier and wire bonded with Al wire as can be seen in Figure 3.13(a). To contact the silicon backside it was scratched with a diamond scriber to get a fresh, unoxidized silicon surface. Then silver paint or silver epoxy was used to glue it on the chip carrier or to create a big conducting pad. The pad or chip carrier ground plate can be contacted by wire bonding.

Devices that were used in liquid were sealed with epoxy. Epoxy was placed manually to cover the bonding wire and pads as shown in Figure 3.13(b). In this way only the lithographically defined leads and the nanowires or nanotubes were exposed to the liquid. As epoxy, Bectron PK 4342 was used for working in aqueous environment or standard solvents and TorrSeal was used to work in benzene and chloroform.



(a) (b)

Figure 3.13: A chip on the chip carrier (a) before and (b) after packaging.

CHAPTER 4

Characterization of SiNW and CNT FETs

Device properties of the SiNW and CNT FETs described in Chapter 3 are discussed here. The silicon substrate is used as back–gate to modulate the conduction of the SiNW or CNT channel. Main focus is put on the small bias regime as this will be used in sensing experiments described in Chapter 5. The two FET types are characterized separately in two sections. A comparison will be given in Chapter 6.

4.1 Silicon Nanowire FET characterization

The main features of Silicon Nanowire (SiNW) FETs can be found in the transfer characteristic, which is the conductance G of the nanowire as function of applied gate voltage V_g as shown in Figure 4.1. Measurements

of the transfer characteristics were always performed at zero dc bias voltage on source–drain, but with a small ac voltage $V_{ac} = 10\,\mathrm{mV}$. In the back–gate configuration the gate voltage is applied via the handle–wafer. At negative back–gate voltages holes are induced in the channel. As the device is p-doped this is the accumulation region. The onset voltage for the accumulation region corresponds to the flat band voltage V_{fb}. It can be found by extrapolating a linear fit of G vs. V_g to zero conductance. The slope of such a linear fit is called transconductance g_m. In the depletion region the current drops exponentially with the gate voltage. A sketch of the charge distribution in these regimes is shown in Figure 4.2. As the nanowire is very thin there is a big region where the conductance is suppressed completely [66]. A further increase of V_g leads to weak and strong inversion with an exponential part and a linear part in the transfer characteristic. The onset voltage of strong inversion is called threshold voltage V_{th}. It can be extracted by a linear fit of G vs. V_g at zero conductance.

Each of these regimes is now described in more details analyzing measurements of conductance vs. back–gate at room temperature and 77 K and current vs. bias measurements. Then the gate capacitance, effects of varying geometry and hysteresis in back–gate response are described.

4.1.1 Accumulation regime

In accumulation the current is proportional to the applied gate voltage (see Equation 2.1)

$$I = \frac{W}{L}\mu C'_{ox}(V_g - V_0)V_{sd} \tag{4.1}$$

with the nanowire width W, length L, the hole mobility μ, the gate oxide capacitance per unit area $C'_{ox} = C_{ox}/A$, the applied gate voltage V_g, an onset gate voltage V_0 and the applied source - drain bias voltage V_{sd}. This relation holds for small bias voltages.

An effective device mobility μ_{dev} at zero bias can be extracted from the transfer characteristic shown in Figure 4.3(a) for room temperature and liquid nitrogen temperature (77 K). In the accumulation regime the slope of a linear fit is given by the derivative of Equation 4.1. Using $G = I/V_{sd}$

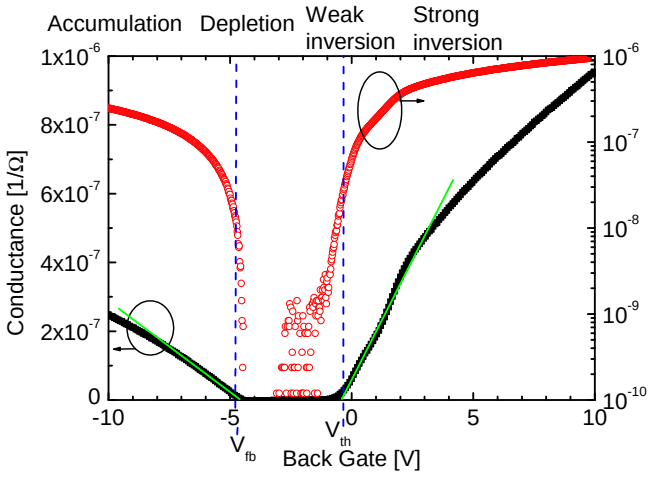


Figure 4.1: Conductance vs. back–gate voltage for a typical SiNW FET of $L = 10\,\mu$m. ■: linear dependance indicated by the left scale, ○: logarithmic dependance indicated by the right scale. V_{sd}: 0 V dc, 10 mV ac (317 Hz).

we get $dG/dV_g = d(I/V_{sd})/dV_g = W/L \cdot \mu_{dev} C'_{ox}$. From this, the hole mobility is

$$\mu_{dev,h} = \frac{L}{W} \frac{1}{C'_{ox}} \frac{dG}{dV_g}. \tag{4.2}$$

With a length $L = 10\,\mu$m of this specific SiNW, a width of 100 nm and the gate capacitance $4.7 \cdot 10^{-4}\,\mathrm{F/m^2}$ as typical value (see Section 4.1.5 for more details), we get

$$\begin{aligned} \mu_{dev,h}(300\,\mathrm{K}) &\sim 100\,\mathrm{cm^2/Vs}, \\ \mu_{dev,h}(77\,\mathrm{K}) &\sim 320\,\mathrm{cm^2/Vs}. \end{aligned}$$

The effective device mobility is higher at 77 K because of reduced electron–

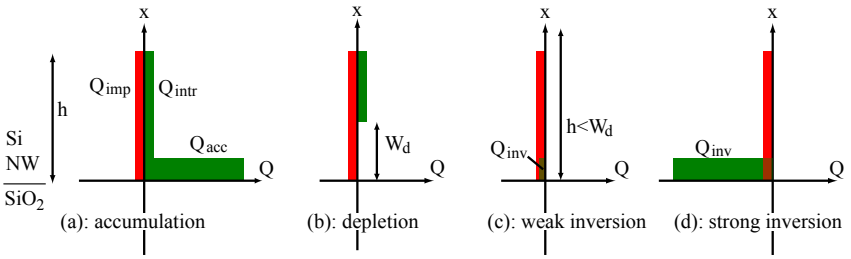


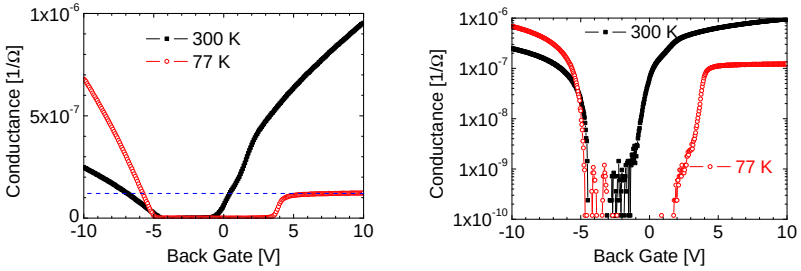
Figure 4.2: Sketch of accumulation, depletion, weak and strong inversion in a SiNW FET of height h. Red marked charges Q_{imp} symbolize immobile charges of the acceptor ions. Green marked charges are mobile and can contribute to a current. Q_{intr}: intrinsic hole charge with $Q_{intr}(V_{fb}) = -Q_{imp}$, Q_{acc} accumulation charge, Q_{inv}: inversion charge with $Q_{inv} < |Q_{imp}|$ for weak inversion.

phonon scattering. The measured device mobility μ_{dev} values are a lower limit for the diffusive hole mobility μ_h. The resistive contribution of the leads are responsible for lower conductance and thus $\mu_h > \mu_{dev,h}$.

At strong negative back–gate voltage, the conductance deviates from the linear behavior as one can best see in Figure 4.1. This can have several reasons:

- For very high fields, there is a dense accumulation layer. This confinement by the transverse electric field leads to a reduced mobility [1, 67].
- The contact resistance of the Al contacts depends on the carrier density. An increase in this series contact resistance might cause a deviation from the linear $G(V_g)$ dependance on the n - side.
- The field distribution (see Section 4.1.5) might depend on the field strength and it might not be completely screened by the SiNW.

The flat band voltage V_{fb} is about $-4.5\,\mathrm{V}$ as deduced by a linear fit indicated in Figure 4.1. The SiNWs are p-doped, but surface depletion



(a) (b)

Figure 4.3: Transfer characteristic of the same sample as Figure 4.1 in (a) linear and (b) logarithmic plot. ■ measured at 300 K, ○ at 77 K.

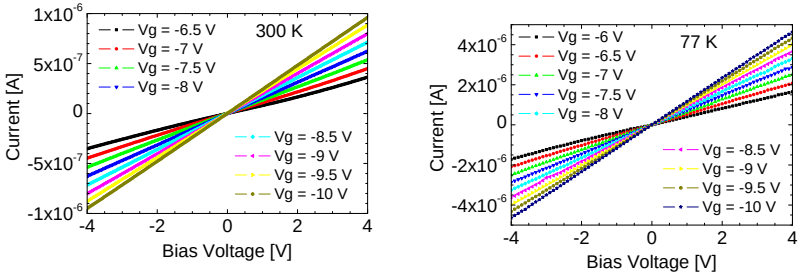
length is much longer than the width and height of the SiNWs so that they are fully depleted and a negative gate voltage has to be applied to reach flat band condition.

In accumulation the current as a function of applied bias voltage is linear for any given gate voltage within the range explored. This is shown in Figure 4.4(a) for a 1 μm long SiNW. In this regime the resistance is ohmic. At 77 K the behavior is linear as well, but for the same gate and bias voltages current is 4 times higher at 77 K because of the increased carrier mobility.

4.1.2 Depletion regime

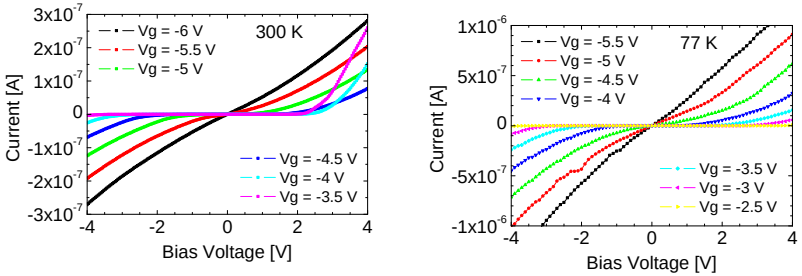
In the depletion regime the nanowire is partially or fully depleted. The current deviates from a linear relation to the applied bias voltage as one can see in Figure 4.5(a). In a fully depleted nanowire the current is suppressed as long as the applied bias voltage is not high enough to inject carriers into the depleted wire.

Thermally activated charges can give rise to a small subthreshold current.



(a) (b)

Figure 4.4: Accumulation: Current vs. bias voltage for a typical SiNW FET of 1 μm length. The applied gate voltages are in the accumulation regime. (a): $T = 300\,\mathrm{K}$ and (b): $T = 77\,\mathrm{K}$, $V_s = -V_d = V_{sd}/2$.



(a) (b)

Figure 4.5: Depletion: Current vs. bias voltage for the same sample as in Figure 4.4. Gate voltages are in depletion regime. (a): $T = 300\,\mathrm{K}$, (b): $T = 77\,\mathrm{K}$.

It decays exponentially with the applied gate voltage with a rate given by the subthreshold swing (Equation 2.7)

$$S = \frac{dV_g}{d(\log(I))}.$$

At constant bias voltage the conductance and the current scale equally and therefore $dV_g/d(\log(I)) = dV_g/d(\log(G))$. The subthreshold swing in the depletion region in the example of Figure 4.1 is

$$S = 110\,mV/dec.$$

Assuming a fully depleted wire we found the expression $S = \ln(10)kT/e(1+C'_q/C'_{ox})$ with $C'_q \to 0$ (Equation 2.11). Including trap states with density D_{it} we get with Equation 2.8

$$S = \frac{dV_g}{d(\log(I))} = (\ln 10)\left(\frac{kT}{e}\right)\left(1 + \frac{e^2 D_{it}}{C_g}\right). \tag{4.3}$$

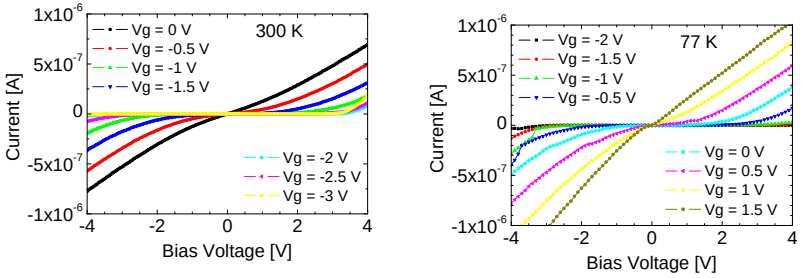
From the measured subthreshold swing the density of interface traps can be calculated

$$e^2 D_{it} \sim 8 \cdot 10^{-5}\,\mathrm{F/m^2}$$

($C_g \sim 1 \cdot 10^{-4}\,\mathrm{F/m^2}$, see Section 4.1.5 for details). This means that for energies within the bandgap ($\sim$1 V) there is one trap state per $\sim 2 \cdot 10^4$ surface atoms. Which is in agreement with low trap state densities reported in high quality SOI wafers [68].

4.1.3 Weak inversion regime

In weak inversion the wire is fully depleted of holes and thermally activated inversion charge is responsible for a small subthreshold current. This small electron current behaves the same way as the subthreshold hole current described in Section 4.1.2. In the example shown in Figure 4.1 the subthreshold swing on the inversion side is about 530 mV/dec. This value is far from the theoretical limit of 60 mV/dec. This could be explained by a higher D_{it} near the conduction band or by a Schottky barrier between



(a) (b)

Figure 4.6: Weak inversion: Current vs. bias voltage for the same sample as in Figures 4.4 and 4.5. Gate voltages are in weak inversion regime. $T = 300\,\mathrm{K}$ in (a) and $T = 77\,\mathrm{K}$ in (b), $V_s = -V_d = V_{sd}/2$.

the Si contact region and the Al contact pad for the case of inversion. The subthreshold swing S is known to increase for Schottky barriers for thick gate oxides as we use here [69].

The threshold voltage V_{th} defines the crossover from weak to strong inversion. It is given by Equation 2.6 as $V_{th} = V_{fb} + 2\Psi_B + Q_s/C_g$. In case of a nanowire, the semiconductor charge Q_s in full depletion corresponds to the charge of acceptor states $Q_s = -Q_{acc} = eN_aWLh$ where N_a is the dopant density and WLh is the nanowire volume. With this the potential of the semiconductor charge is $Q_s/C_g = heN_a/C'_g$. Considering interface traps the threshold voltage is given by [66]

$$V_{th} - V_{fb} = 2\Psi_B + \frac{qN_a}{C'_g}h + \frac{e^2D_{it}}{C'_g} \cdot 2\Psi_B$$

where D_{it} is the number of interface traps per unit area and per energy. The bulk potential Ψ_B of silicon with a doping level of $10^{15} - 10^{16}\,\mathrm{cm}^{-3}$ is about $0.2-0.3\,\mathrm{eV}$ [1]. With all this we can estimate the density of interface traps to be $e^2D_{it} \sim 9 \cdot 10^{-5}\,\mathrm{F/m^2}$. This is very well in agreement with the value obtained from the subthreshold swing in Section 4.1.2.

For high bias voltages the current behaves in analogy to the depletion region. This can be seen in Figure 4.6.

4.1.4 Strong inversion regime

In strong inversion there is a thin layer of electrons induced at the interface of the nanowire with the buried oxide. This induced charge Q_i is much bigger than the depletion charge and therefore we can consider the simple relation $Q_i = C(V_g - V_{th})$ for $V_g > V_{th}$. The physics is the same as in the accumulation region.

From the transfer characteristics in Figure 4.3(a), the electron mobility can be estimated from Equation 4.2 in analogy to the hole mobility. By using a linear fit on the n side we get

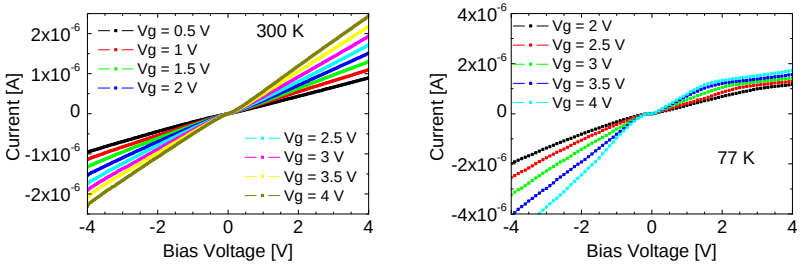
$$\mu_e(300\,\mathrm{K}) = 320\,\mathrm{cm}^2/(\mathrm{Vs}).$$

This is about three times larger than the hole mobility. This is equal to the ratio between electron and hole mobility in bulk silicon

$$\mu_e/\mu_h = 3.$$

This indicates that holes and electrons see equal series resistances in the leads and contacts.

At 77 K the conductance is limited at high gate voltages to $\sim 1.2{\cdot}10^{-7}\,1/\Omega$ (see Figure 4.3(a)). An explanation can be found from the bias dependance: The current versus applied bias is plotted in Figure 4.7 for the same device as in Figure 4.4. At room temperature the current depends linearly on the voltage (Figure 4.7(a)). But at lower temperature there is a barrier for small bias voltage as one can see in Figure 4.7(b). Such a barrier is expected as Al tends to make a Schottky barrier to electrons in silicon. In the particular case of Figure 4.7(b) the asymmetric behavior indicates that the electron current is limited at one of the contacts in case of high gate and voltage bias. This effect might come from a p-n junction between the inverted leads and a local p-region at one of the contacts coming from p-doping by Al.



(a) (b)

Figure 4.7: Strong inversion: Current vs. bias voltage for the same sample as Figures 4.4 - 4.6. Gate voltages are in strong inversion regime. $T = 300\,\mathrm{K}$ in (a) and $T = 77\,\mathrm{K}$ in (b).

The transfer characteristic in the inversion regime varies much between devices of different fabrication runs. Some show current limitation for higher gate voltage at room temperature, others at 77 K only. This suggests that on the n-side, a mechanism is limiting which is very sensitive to fabrication details. Most delicate are surface and interface effects. Possible explanations are Schottky barriers between Al pads and silicon contact region, surface state induced Fermi level pinning or surface dominated conduction.

The accumulation side is much more robust and does not suffer from such effects. For this reason we set the main focus on the accumulation side, especially in the context of sensing in Chapter 5.

4.1.5 Capacitance of gate coupling

As described before, the charge induced in the channel can be related to the applied gate voltage by $Q_{ind} = C_g\,(V_g - V_0)$, where V_0 is V_{th} or V_{fb} in case of inversion or accumulation. The gate potential $V_g - V_0$ is split in the potential drop Ψ_{sub} over the depletion region in the handle layer, the

potential drop Ψ_{ox} over the gate oxide and the potential drop Ψ_{nw} in the nanowire. This is sketched in Figure 4.8. The field lines indicate that in addition to the field penetrating through the gate oxide into the nanowire there is some field penetrating the sidewalls. In this section we will see that the total capacitance $C_g(V_g)$ can depend on the applied voltage. One can write the total capacitance as a series capacitance $1/C_g = 1/C_{ox} + 1/C_{d,nw} + 1/C_{d,sub}$ with

C_{ox}**:** the capacitance given by the gate oxide and the nanowire geometry,

$C_{d,nw}$**:** the depletion capacitance in the nanowire,

$C_{d,sub}$**:** the depletion capacitance in the substrate.

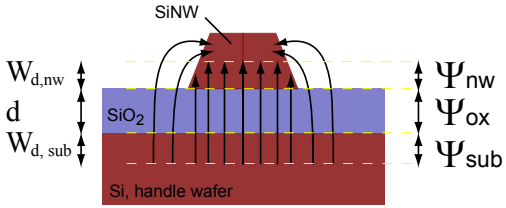


Figure 4.8: The electric field applied to the back–gate of a SiNW FET structure drops over the substrate depletion layer by a part Ψ_{sub}, over the oxide by a part Ψ_{ox} and over the depletion layer in the nanowire by a part Ψ_{nw}.

To calculate C_{ox} we consider the case of zero depletion on both sides, substrate and nanowire as if they would be metallic. In this case the total capacitance does not depend on the applied gate voltage and is given by pure geometric considerations. The gate oxide capacitance can be estimated in first approach by $C'_{ox} = C_{ox}/A = \varepsilon_0\varepsilon_{SiO_2}/d = 2.3 \cdot 10^{-4}\,\mathrm{F/m^2}$ for 150 nm thick oxide. This is a lower bound as only field lines perpendicular to the oxide are considered, but the field can penetrate the wire all around. A more detailed study considering a conducting wire lying on an oxide surface can be found in [18, 19]. An analytical expression

can be given for a metallic wire of radius r embedded in a dielectric ε_r on a infinite metal plate in distance d: $C'_{ox} = \varepsilon_0\varepsilon_r / \ln(2(d+r)/r)$. In our case the nanowire is lying on silicon oxide and is surrounded by air. This leads to a smaller effective dielectric constant $\varepsilon_r^{eff} \sim \varepsilon_{SiO_2}/2 \sim 2$ [18, 19]. With such an effective dielectric constant, the capacitance is

$$C'_{ox} = 4.7 \cdot 10^{-4}\,\mathrm{F/m}^2$$

for a geometry corresponding to our devices (wire of 60 nm height and 100 nm width on a 150 nm oxide layer). Detailed numerical calculations by Wunnicke [18] and by Vashaee [19] for rectangular or triangular wire geometry give values that differ by 10 % at most. Note that the capacitance per unit area is larger for the wire than for the leads and contacts.

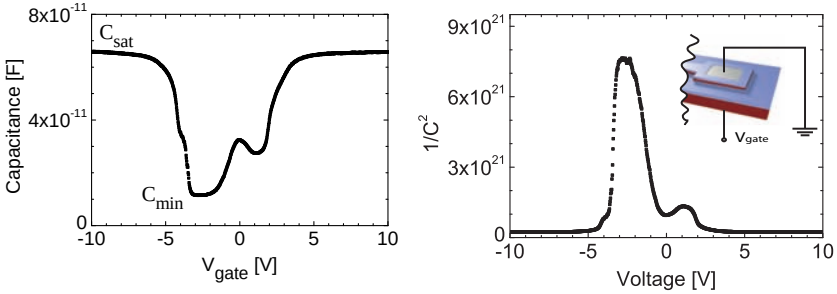
In a semiconductor an applied voltage can lead to a depletion layer W_d. The corresponding depletion capacitance is given by

$$C_d = A\frac{\varepsilon_{Si}\varepsilon_0}{W_d} \tag{4.4}$$

with area A and depletion width W_d. In the following two paragraphs we will discuss the depletion capacitance of the nanowire and the substrate.

The depletion capacitance of the nanowire contributes most if the nanowire is fully depleted — which leads to the smallest capacitance. A lower bound of this capacitance can be estimated by inserting the wire height h into Equation 4.4: $C^{min}_{d,nw}/A > \varepsilon_{Si}\varepsilon_0/h \simeq 2 \cdot 10^{-3}\,\mathrm{F/m}^2$.

The depletion capacitance of the substrate can be measured as schematically shown in the inset of Figure 4.9(b). For a complete device, the capacitance between the device layer and the substrate is measured as function of the applied gate voltage. A dc voltage with ac modulation of 11 kHz was applied to the gate and the capacitive part of the current flowing to the grounded contact was measured. At high gate voltages, if the substrate is in accumulation or inversion, the charge layer is very thin and the total capacitance is given by the oxide capacitance. For small bias voltages the substrate is in depletion and $C_{d,sub} = A\varepsilon_{Si}\varepsilon_0/W_{d,sub}$ is small and the total capacitance is reduced. The minimal depletion



(a) (b)

Figure 4.9: Back–gate spectroscopy on a SiNW FET device. (a) shows the capacitance as function of applied back–gate voltage. In (b) $1/C^2$ is plotted. The inset shows the setup.

capacitance of the substrate can be calculated with the saturation capacitance C_{sat} and the minimal capacitance C_{min} from Figure 4.9(a) by $1/C_{d,sub}^{min} = 1/C_{sat} - 1/C_{min}$. This gives $12\,\mathrm{pF} \triangleq 6 \cdot 10^{-5}\,\mathrm{F/m^2}$ using the total device area of $2 \cdot 10^{-7}\,\mathrm{m^2}$. This gives a depletion width of

$$W_{d,sub} = 0.7\mu\mathrm{m}.$$

The depletion width is given by (see Equation 2.4)

$$W_d = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0(\Psi_s - V)}{eN_a}}$$

with the doping density N_a, surface potential Ψ_s and the applied voltage V. As $W_{d,sub} \gg W_{d,nw}$ we use a simplified sum $1/C = 1/C_{ox} + 1/C_{d,sub}$. Combining this with Equation 4.4 we get

$$\frac{1}{C_{d,sub}} = \frac{1}{C} - \frac{1}{C_{ox}} = \frac{1}{A}\sqrt{\frac{2}{e\varepsilon_S N_a}(\Psi_s - V)}$$

$$\frac{1}{C} = \frac{1}{A}\sqrt{\frac{2}{e\varepsilon_S N_a}(\Psi_s - V)} + \frac{1}{C_{ox}}$$

$$\frac{1}{C^2} \simeq \frac{2}{A^2 e \varepsilon_S N_a}(\Psi_s - V), \qquad C_{ox} \gg C_d \tag{4.5}$$

This is the quantity plotted in Figure 4.9(b). By a linear fit on the plot of $1/C_{tot}^2$ versus voltage in accumulation for substrate we can get the dopant density

$$N_a \sim 2 \cdot 10^{15}\,\mathrm{cm}^{-3}$$

from Equation 4.5 (note: in depletion we assume the nanowire not to be conducting so that the effective area is given by one contact and lead). This value corresponds to the lower end of the specification $10^{15} - 10^{16}\,\mathrm{cm}^{-3}$ of the wafer supplier.

If we want to know the total capacitance of the gate coupling to the nanowire C'_g, we have to calculate the total capacitance of the series capacitance as evaluated above: $1/C'_g = 1/C'_{ox} + 1/C'_{d,nw} + 1/C'_{d,sub}$. For a nanowire $C'_{ox} = 4.7 \cdot 10^{-4}\,\mathrm{F/m^2}$ as previously calculated. We neglect the $1/C'_{d,nw}$ term as it is much smaller than the others. $C'_{d,sub}$ is calculated by $1/C'_{d,sub} = A \cdot (1/C_{sat} - 1/C(V))$ from Figure 4.9 and is $> 6 \cdot 10^{-5}\,\mathrm{F/m^2}$. With all this the total capacitance is

$$C'_g \simeq 6 \cdot 10^{-5} - 4.7 \cdot 10^{-4}\,\frac{\mathrm{F}}{\mathrm{m}^2}.$$

The gate capacitance C'_g is large in the regions where the nanowire is in accumulation and inversion and is smaller for small gate voltages because in this region a depletion layer forms in the substrate. In depletion a mean gate capacitance of $C'_g \sim 1 \cdot 10^{-4}\,\mathrm{F/m^2}$ is assumed generally (for example in previous estimations of the doping level and the interface trap state density).

4.1.6 Geometrical consideration

To compare depletion effects of the thin SOI device layer to our nanowires the device layer of an unstructured SOI wafer was tested when a gate voltage was applied via back–gate. The outcome is shown in Figure 4.10. In a first experiment, the oxide on the device layer was freshly etched by

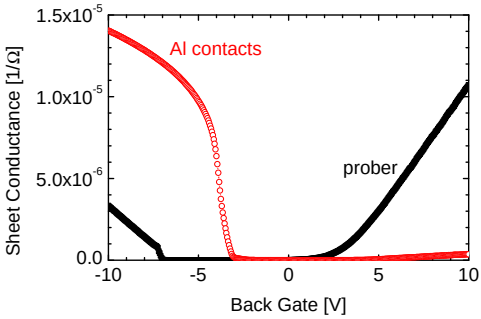
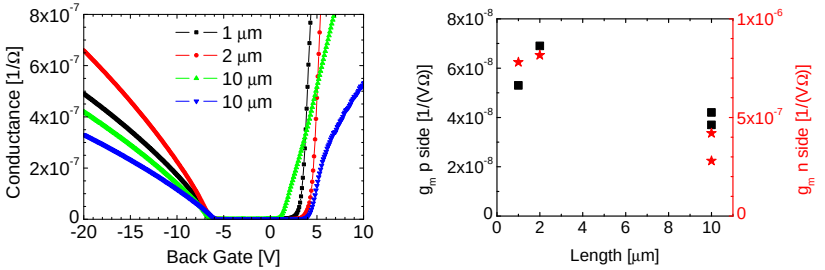


Figure 4.10: SOI wafer pseudo MOSFET: Device layer of SOI wafer was contacted by prober needles of tungsten carbide (■) or Al pads (○). Gate voltage was applied via back–gate.

buffered HF and then contacted with prober needles of tungsten carbide. In a second experiment, contact pads of 200 μm × 200 μm were defined by photo–lithography. The oxide was removed, Al evaporated and the contacts annealed as it was done for the transistors (see Chapter 3). The contact separation in both cases was in the range of 1 mm, the unstructured device layer was much larger. For such a geometry a conversion factor 4/3 has been reported [68] to deduce the sheet conductance $G_{\square} \simeq 4/3 \cdot I/V_{sd}$. Although this is not an exact measure it can give some insight and is therefore plotted in Figure 4.10. This graph shows that there is a barrier for holes in case of prober needles and a barrier for electrons in case of Al contacts. Threshold voltages depend on the barrier as expected for Schottky barrier transistors. On the n-side of the Al contacted device layer the current is of the same order as in highly conducting NWs. Contact barriers on the n-side and typical NW resistances are obviously of the same order of magnitude. For Al contacts, the p-side seems to be barrier free so we can assume that the observed threshold voltage corresponds to the flat band voltage V_{fb}. It is shifted slightly less to negative voltages as it is for SiNW FETs (see for example Figure 4.1). Thus we can conclude that surface depleting on the sidewalls of the nanowire is responsible for

a shift in the order of $\sim -1\,\mathrm{V}$. Using the same geometrical argument as above the hole mobility can be extracted from a contacted device layer using Equation 4.2 by replacing L/W by a constant factor of 4/3 [66]. With the oxide capacitance $C'_{ox} = 2.3 \cdot 10^{-4}\,\mathrm{F/m^2}$ from Section 4.1.5 we get $\mu_h = 4/3 \cdot 1/C'_{ox} \cdot dG/dV_g \simeq 220\,\mathrm{cm^2/(Vs)}$. This is slightly higher than the best device mobilities μ_{dev} observed for nanowires which shows that scattering at the nanowire side-walls contribute to lower device mobility. It is still below bulk silicon mobilities meaning that surface scattering at the oxide interfaces plays an important role.

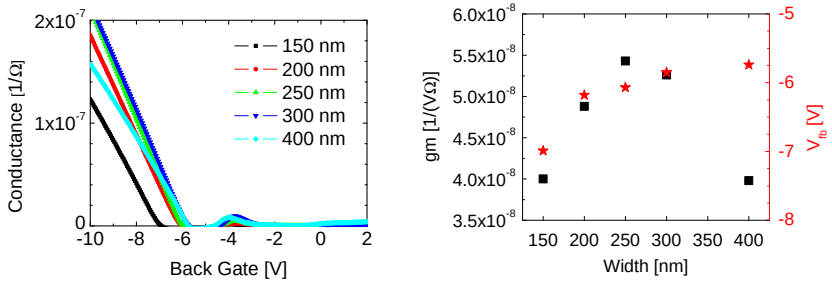


(a) (b)

Figure 4.11: Transfer characteristics (a) of SiNW FETs of various NW lengths. The width was $\sim 100\,\mathrm{nm}$ and the length was designed to 1, 2 and $10\,\mu\mathrm{m}$. (b) shows the transconductance g_m for p- (■) and n-side (★).

SiNW FETs of different length and width were fabricated to study geometrical effects. For thin nanowires ($\sim 100\,\mathrm{nm}$) three lengths L were compared: $1\,\mu\mathrm{m}$ and $2\,\mu\mathrm{m}$ and $10\,\mu\mathrm{m}$. Transfer characteristics for these devices are shown in Figure 4.11(a). The transconductances $g_{m,p}$ and $g_{m,n}$ are plotted versus the wire length in Figure 4.11(b). For an ideal nanowire FET the transconductance $g_m = dG/dV_g$ is expected to scale with $1/L$ (see Equation 4.1). Resistive contributions from contacts and leads reduce this dependance. For short nanowires of $1\,\mu\mathrm{m}$ or $2\,\mu\mathrm{m}$ one cannot see any clear length dependance in general (see Figures 4.11(b)

and Appendix B.1). For such short wires the resistance of the wire is smaller than the resistance of the leads. 10 μm long nanowires show clearly smaller transconductance in both, accumulation and inversion region. The transconductance of 10 μm wires is around $1.5 - 3$ times smaller than of short ones (1 μm and 2 μm), which is significantly less then the length ratio.



(a) (b)

Figure 4.12: (a) Transfer characteristics of SiNW FETs with widths varying between $\sim 150 - 400$ nm. $L = 10\,\mu$m. (b) shows the transconductance g_m of p-side (■) and V_{fb} (★) deduced from (a), both bs. NW width.

The transconductance g_m for long nanowires ($\sim 10\,\mu$m) with varying widths is plotted in Figure 4.12. In accumulation the transconductance increases with increasing width from 150 nm to 250 nm by a factor 1.3 almost reaching the expected 1.5. But it does not increase any further for wider nanowires as the series resistance of leads start to dominate. The flat band voltage V_{fb} is plotted as a function of width in Figure 4.12(b) on the right scale (★). It shifts to more negative values for thinner wires up to a maximum shift of ~ 1.2 V which corresponds to the observation on a SOI wafer pseudo MOSFET described above. This shift is caused by surface depletion of the sidewalls.

From the above observations we deduce, that in device designing the resistive contributions of the leads, that get more narrow towards the nanowire,

have to be considered. The leads are of the same doping level as the nanowire so their resistance varies with applied gate voltage in analogy to the nanowire. In a first approach their contribution can be described by an increase in effective wire length $L_{eff} > L$. Note that this is only a rough description for two reasons. First they have a less strong capacitive coupling to the gate as they are wider than the narrow nanowires (see discussion in Section 4.1.5 for gate coupling). Second, as they are wider, less gate voltage has to be applied to reach accumulation in the leads than in the NW. For long and thin enough wires lead resistances are not dominating. Reducing the length below 10 μm is only recommended if the width can be reduced with high reproducibility fare below 100 nm to be sure that contributions of the leads are small.

To study the effect of the top oxide on a SiNW FET, the transfer characteristics were measured before and after removing the top oxide. During the fabrication process the oxide mask was thinned to $\sim$ 40 nm by CHF_3 plasma before etching the silicon device layer. After first test measurements, a 10 μm wide channel is patterned on top of the nanowire by photo–lithography in the region depicted in the right panel of Figure 4.13. The rest of the top oxide was removed by buffered HF. The transfer characteristics are shown in Figure 4.13(a). The most obvious effect is that the conductance saturation at high gate voltage is lifted. As the top oxide was removed only locally on the narrow wire this cannot be a contact effect. We suggest that the NW level is pinned by the top oxide.

4.1.7 Hysteresis

When the gate voltage is swept from negative to positive voltages and backwards, a hysteresis in conductance response can occur. Such a hysteresis is often observed, usually on p- or n side, sometimes on both sides. At 77 K hysteretic effects are frozen out as shown in Figure 4.14(a). To ensure clean NW side wall surfaces a working and packaged device was shortly etched with buffered HF and TMAH. After such an etching procedure, the hysteresis effect is basically gone as one can see in the example of Figure 4.14(b). This shows that surface effects on the sidewalls of the nanowire are responsible for hysteretic effects.

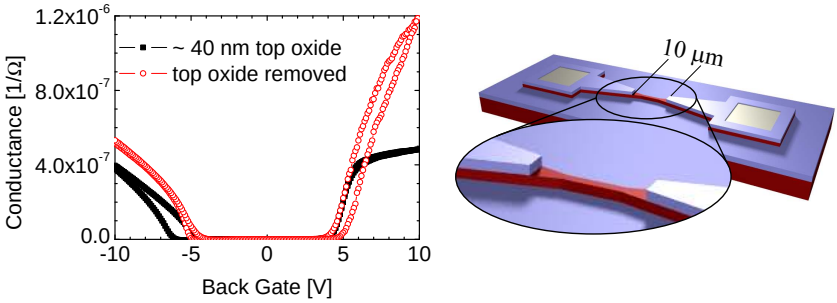
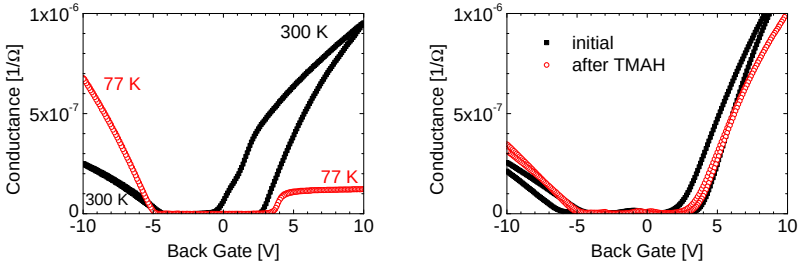


Figure 4.13: Transfer characteristics of a SiNW FET with and without top oxide ($L = 1\,\mu$m, $W \sim 100\,$nm). The oxide was removed within a $10\,\mu$m wide channel on top of the NW and adjacent leads as sketched in the drawing.



(a) (b)

Figure 4.14: Hysteresis in conduction as function of gate voltage for two SiNW FETs. In (a) the hysteresis is frozen out by low temperature, in (b) the hysteresis was removed by etching the device with buffered HF dip and and about 10 min in TMAH (25% plus 10% isopropanol in H_2O).

4.1.8 Summary SiNW FETs

In summary we can say that the SiNW FETs designed as described in Chapter 3 show both, accumulation and inversion conduction. In long ($> 10\,\mu$m) and thin ($< 100\,$nm) nanowires the current is limited by the NW channel for a temperature of 300 K. In both regions the current is linear with the bias voltage in a wide range. Ambipolar SiNW FETs that are not dominated by Schottky barriers could be realized thanks to the large contact region and semiconducting leads. A slightly higher doping of the device layer would reduce $V_{th} - V_{fb}$ and improve the transparency of the Al – Si contacts and thus reduce the observed variation between different devices in the inversion regime. The accumulation regime is very robust regarding threshold and linearity versus back–gate. There is no intrinsic hysteresis in the transfer characteristic of the device. Typical values for the device parameters discussed in this section are shown in Table 6.1 in comparison to CNT FETs.

4.2 Carbon Nanotube FET characterization

To characterize the effect of an applied electric field on the conductance of a carbon nanotube, a gate voltage was applied to the silicon substrate (back–gate) and the current through the tube was measured at a small constant ac voltage of typically $1-10\,$mV. A plot of measured conductance vs. applied gate voltage is shown in Figure 4.15. The most important features indicated in the graph are:

V_0 is the threshold voltage for up and down ramp. Up ramp means running the gate voltage from negative to positive voltage, down ramp means running the gate from positive to negative voltages. The threshold voltage tells us at which voltage the transistor "switches on". It is deduced from measurements by the intersect of a linear fit dG/dV_g with $G = 0$. (Note that in the theory Section 2.3.2 V_0 was defined differently.)

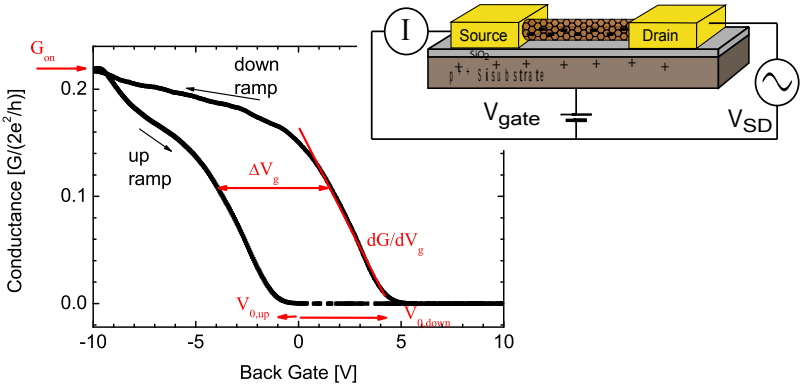


Figure 4.15: Typical conductance vs. applied back–gate voltage of a SWNT FET. Bias 1 mV, 317 Hz. Indicated are the threshold voltage V_0 for up and down ramp, the on-conductance G_{on}, the hysteresis ΔV_g and the transconductance dG/dV_g. Inset: scheme of CNT FET measurement.

G_{on}, called the on-conductance, is the value of conductance saturation for low gate voltages. For practical reasons the conductance value at $V_g = -10\,\mathrm{V}$ is usually chosen.

dG/dV_g in the linear region is called transconductance g_m. It measures the efficiency of the gate response.

ΔV_g is the hysteresis between up and down ramp. To ensure that the hysteresis does not depend on initial conditions, the gate was swept slowly to the initial value. Typically ten gate ramps were recorded and averaged.

In the next four subsections these features are examined in more details.

4.2.1 Threshold voltage

The threshold voltage varies quite a lot from device to device. Values in the range of

$$V_0 = -5 \ldots 9\,\mathrm{V}$$

have been observed. Ideal CNTs would be intrinsic semiconductors, but in general CNT FETs are p-type. Two possible reasons are mentioned in literature. The first one is a possible electron transfer from the semiconducting CNT to the metallic contacts [70] and alignment of the valence band to the metal Fermi level due to a work function difference. The second one is the adsorption of oxygen or water molecules on the nanotube surface which would lead to an effective charge transfer to the nanotube [71]. n-type conduction is possible when doping the nanotubes [72, 73] or when using contact metals with low work function. Schottky barrier dominated devices can show both conduction types [31].

4.2.2 On-conductance

At negative gate voltages the resistance of the nanotube channel is very low and the overall resistance is dominated by the quantum resistance

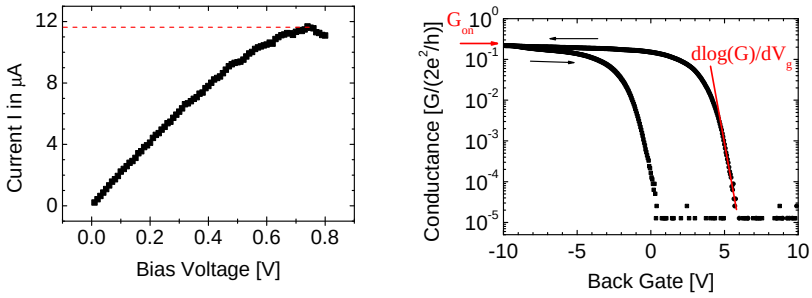


Figure 4.16: (a) Current vs. bias voltage for a SWNT. (b) Logarithmic plot of conductance vs. back–gate voltage of the same device as in Figure 4.15

and by the contact resistance between the metal leads and the CNT (see Equation 2.18 and Appendix A.2.1). This saturation conductance varies from device to device but mostly lies in the range of

$$0.1 - 1 \cdot 2e^2/h$$

(contact separation $L = 0.5 - 1\,\mu$m, $V_{sd} = 1\,$mV). Note that typical values reported in literature are in the range of $0.01 - 0.1 \cdot 2e^2/h$ [74, 75, 52, 28], but values as high as $2e^2/h$ have been reported by the group of H. Dai [25] ($L = 300\,$nm). The high G_{on} shows that our devices have small contact barriers and thus small Schottky barriers [20]. At large bias the current saturates at a value of around $10 - 25\,\mu$A as shown in Figure 4.16(a). Scattering on optical phonons has been reported [76, 77] as the main reason for this saturation. If bias is driven further nanotubes will break due to current-induced defect formation [78] that can lead to local oxidation.

4.2.3 Slope in transfer characteristic

There are two main measures for the dependance of the conductance on the applied gate voltage. One for the regime above threshold and a second below. Above threshold the strength of the gate response can by described by the slope of the transfer characteristics dG/dV_g. From Chapter 2.3.2 we know the expression(Equation 2.19)

$$\frac{dG}{dV_g} = \frac{\mu}{L}\frac{C_{ox} \cdot C_{NT}}{C_{ox} + C_{NT}}.$$

For a measure that accounts for the device geometry, quantum capacitance and series resistances, we can define an "effective device mobility" [24]:

$$\mu_{dev} = \frac{L}{C_g}\frac{dG}{dV_g} \tag{4.6}$$

We look at μ_{dev} in linear regime only. With the gate capacitance $C_g^\star \sim 20\,\mathrm{pF/m}$ (see Equation 2.12) we get from a linear fit on the transfer characteristics in Figure 4.15 an effective device mobility of

$$\mu_{dev} = 1500\,\mathrm{cm^2/(Vs)}.$$

We measured mobilities up to $2500\,\mathrm{cm^2/(Vs)}$. The intrinsic mobility μ of a nanotube is expected to be higher than this value, as screening by the metal contacts reduces the gate efficiency and contact resistances damp the device conductance. Still the observed values agree with mobility values for Schottky barrier free devices with a tube diameter of the order of 1.5 nm and $L = 10\,\mu$m as reported by Zhou [79]. Phonon scattering decreases for increasing diameter. Therefore higher values are predicted by [80] and have been reported for CNT devices with big ($d > 3\,\mathrm{nm}$) CNTs and higher bias [24, 79, 25]. Device mobilities of contact dominated devices are much lower (see for example [51]).

In the subthreshold region the conductance depends exponentially on the gate voltage as can be seen in Figure 4.16(b). The subthreshold swing S is defined to express which gate voltage is needed to suppress the conductance by one order of magnitude. In Section 2.3.2 we found Equation

2.20 for the subthreshold swing

$$S = \frac{dV_g}{d(\log(G))} = \ln 10 \frac{kT}{e} \frac{1}{\alpha}.$$

For the CNT FET in Figure 4.16(b) we find

$$S = dV_g / d\log(G) = 570\,\mathrm{mV/dec}.$$

This value is far above the theoretical limit of 60 mV/dec for a capacitance ratio of one. In a channel limited device with thick gate oxide and wide metal contacts the field is partially screened by the contacts [81]. This leads to a efficiency factor α below 1. If Schottky barriers dominate the subthreshold slope S depends strongly on the gate oxide as mentioned in Section 2.3.3. For 400 nm SiO_2 as used in our devices it is expected to be larger [82]. For Schottky barrier dominated devices [20], $S \sim 2000\,\mathrm{mV/dec}$ was reported for 120 nm SiO_2 [17]. For SiO_2 of 20 nm, Schottky barriers lead to an increase in S of more than a factor two [22], and this effect is more pronounced for thicker oxides [28]. This tells us that our devices are not governed by Schottky barriers.

4.2.4 Hysteresis

There is a significant hysteresis between up an down ramp of the gate voltage. This is one of the main problems when working with CNT transistors in general. The width of the hysteresis depends on the speed of gate ramp as one can see in Figure 4.17. The hysteresis is smaller for fast gate ramps. The plot of hysteresis as a function of gate ramping speed shows that the hysteresis increases dramatically for slow gate ramps. For an estimation of the timescale an exponential decay was used to fit the hysteresis vs. ramp speed. This gives a typical time scale of 0.6 V/s. Trap states in the SiO_2 [83, 52, 84] or ions [85] and water [86, 87] adsorbed on the nanotube surface and SiO_2 surface were reported to be responsible for this hysteresis effect. To lower the energy of oxide trap states [83] samples were illuminated with UV light (356 nm). The hysteresis is generally not affected (or even slightly increased in this specific case) which indicates that in our devices this is not the dominant effect (see Figure 4.18(a)).

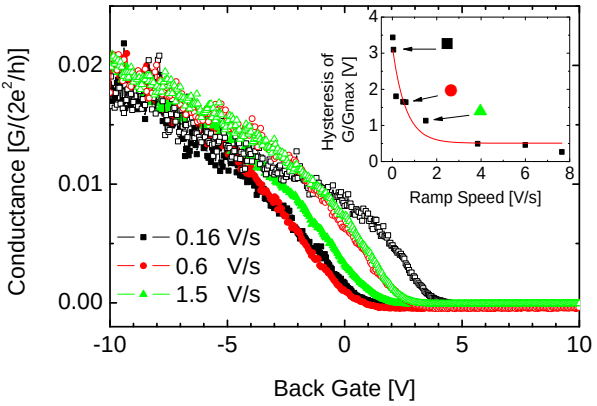


Figure 4.17: (a) Conductance vs. back–gate voltage of a SWNT device with varying sweeping speed. The hysteresis is measured by the difference of the area below the down ramp (open symbols) and the up ramp (solid symbols), divided by the maximum conductance. Inset: the hysteresis vs. ramp speed.

To make the oxide surface hydrophilic it was covered with a monolayer of alkanetriethoxysilane with methyl or octyl as alkane-chain as described in the Appendix C.6. The hysteresis is not reduced by this treatment (more details in Section 5.6.2). This shows that the hydrophilicity of the NT environment is not the main effect of the hysteresis. This is in contrast to reports of McGill [52] who made a hydrophobic surface by an octadecyltrichlorsilane monolayer before deposing CNTs from liquid and contacting them. He reported very low hysteresis. The difference is that in our case adsorbates, for example water molecules, between the nanotube and the metal leads or in proximity could play an important role. In [52] this effect is ruled out because the surface is hydrophobic before contacting the CNTs. To minimize the amount of water adsorbed

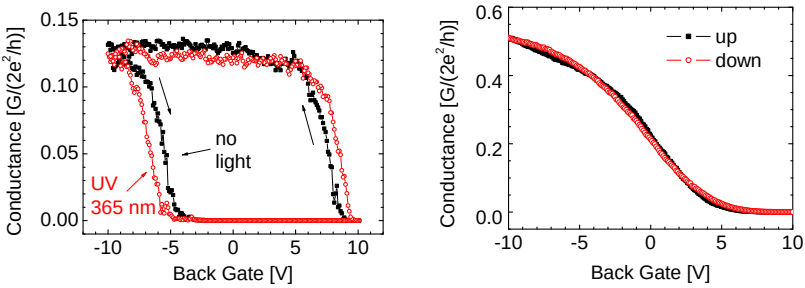
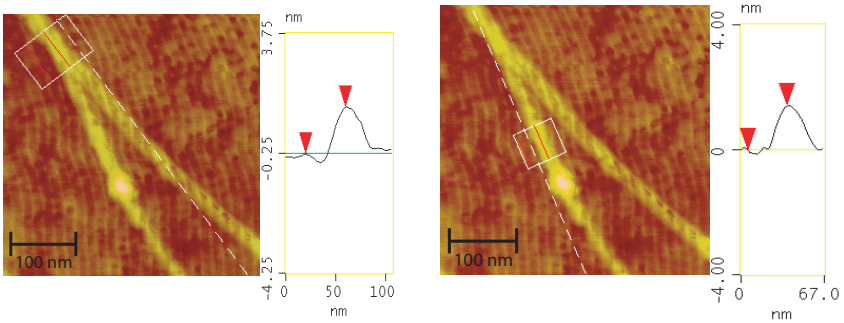


Figure 4.18: (a) G vs. V_g on a SWNT FET with high hysteresis. The effect of UV light (365 nm) illumination (○) is very small. (b) G vs. V_g on a SWNT prepared by vacuum annealing at 130° C, $1 \cdot 10^{-6}$ bar for 22 hours before deposition of Pd contacts. Hysteresis is dramatically reduced.

in the contact region, the devices were annealed in vacuum (10^{-6} mbar) at 130° C overnight before evaporating the metal contacts. Resulting devices showed very low hysteresis as one can see in the example of Figure 4.18(b). This might be a way to produce CNT FETs with low hysteresis. Further studies are needed to learn about this effect in details. Therefore it would be important to anneal devices in situ before evaporating.

4.2.5 Bundles versus individual nanotubes

Carbon nanotubes have a strong tendency to bundle, not only if they are in suspension but even if growing on a substrate. Big bundles can easily be recognized by AFM or even by SEM. In Figure 3.10 such bundles can be seen. But bundles can be extremely small so that they even cannot be recognized by AFM. An example of such a bundle is shown in Figure 4.19. From the cross Section in the left part one would expect an individual SWNT of diameter 1.6 nm. But it branches and two resulting tubes can be seen that are bundled in the upper left part of the image. The apparent



(a) (b)

Figure 4.19: AFM pictures (tapping mode) of CNTs grown by CVD with ethylene (Fe catalyst). The apparent height of the bundle (a) is 1.6 nm (top left corner) is almost exactly the same as that of the tube in (b) with 1.5 nm (lower tube).

diameter of an individual tube is about 1.5 nm. This shows that from images we cannot unequivocally conclude to have an individual SWNT. Electrical characterization has to be performed.

In a bundle of carbon nanotubes there are metallic tubes in parallel to semiconducting ones. When conductance through the semiconducting tubes is suppressed there is a high background conductance of metallic tubes. In addition the gate coupling might be reduced if the metallic tubes screen the field. An example of the back–gate response of a bundle and an individual tube is shown in Figure 4.20 in logarithmic scale. Where as the conductance of the SWNT can be suppressed by orders of magnitude, the conductance of the bundle is suppressed to about a 1/3 of the maximum value. This is the reason why it is important to have FETs of individual tubes for sensing.

In Section 4.2.2 the current saturation for high bias is described for a SWNT. In a bundle the maximal current is expected to be higher as it can be distributed by the different tubes. The contact resistance between

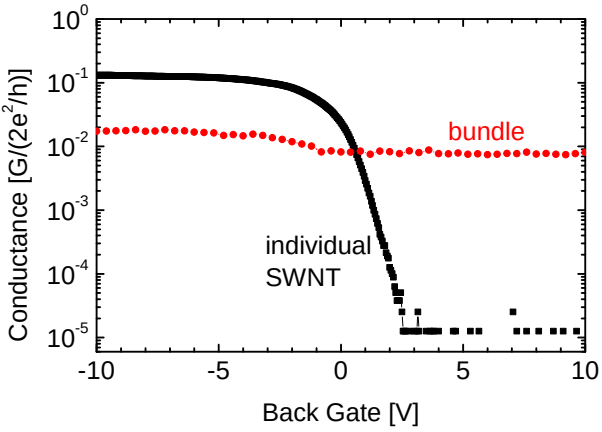
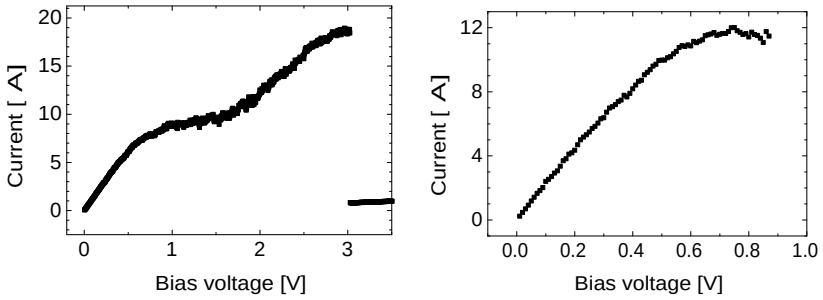


Figure 4.20: Transfer characteristic of FETs made of a bundle and an individual SWNT.



(a) (b)

Figure 4.21: Current vs. bias voltage for a CNT bundle (a) and an individual tube (b).

the metal contact and the different tubes of a bundle varies quite a lot. Therefore one expects that the one tube with the smallest contact resistance carries most of the current. When it comes into saturation, other tubes start to contribute. Therefore a step like behavior is expected. These features can be seen in Figure 4.21. The current as function of applied bias of a bundle is shown in (a) whereas (b) shows the typical behavior of an individual tube. Note that the CNT bundle is destroyed at 3 V bias.

Electrical measurements cannot distinguish between small bundles of SWNTs or thin multi–walled carbon nanotubes. When CVD growth was performed with ethylene as feeding gas multi–walled nanotubes were very common (see Appendix C.2). This gives similar FET characteristics. For CVD with methane SWNTs are expected for the growth parameter we used [63]. Bundling during CVD could be avoided to a large extend as described in Appendix C.2.

4.2.6 Summary CNT FETs

The CVD and device fabrication scheme described in Chapter 3 has proven to lead to high quality FETs. We summarize:

- High contact transparency is achieved leading to
  - high on–conductance in the range of $0.1 - 1 \cdot 2e^2/h$,
  - high effective device mobility $\mu_{dev} : 100 - 2500\,cm^2/(Vs)$,
  - low subthreshold swing ($< 200\,mV/dec$) for 50 % of the devices.
- The all present issue of hysteresis in back–gate response is addressed. As an important origin the contact region has been identified. To reduce hysteresis we suggest to anneal the devices before evaporating the contact metal.
- High certainty to contact unbundled tubes is gained by a combination of imaging, transfer characteristic and bias dependance.

CHAPTER 5

Environmental Effects on Nano FETs

5.1 Introduction

5.1.1 Chemical sensors on basis of MOSFETs

The most common chemically sensitive field-effect transistor is the Ion Sensitive Field Effect Transistor (ISFET) introduced independently by Bergveld [88] and by Matsuo et al. [89]. It consists of a standard MOSFET with the gate electrode replaced by an electrolyte solution and electrode as shown in Figure 5.1. The channel resistance depends on the potential at the gate oxide. This potential depends on the electrode potential V_{el}, the liquid interface potentials and the surface charge of the insulator – liquid interface Ψ_i. The deposition of ions at the insulator surface is equivalent to a change of electrolyte–gate potential V_{el}. The effective gating comes

from a superposition $V_{el} + \Psi_i$. In this case the ISFET is treated as a MOSFET and the conductance is monitored as function of V_{el}. A change in Ψ_i leading to a shift in $G(V_{el})$. This effect can be expressed by a shift in the flat band voltage V_{fb}.

The expression $V_{fb} = \phi_m - \phi_s - Q_{ox}/C_g$ (Equation 2.2) for the flat band voltage in a standard MOSFET has to be adapted to the situation of electrolyte–gate. The metal work function ϕ_m is replaced by the work function of the electrode – solution interface ϕ_{sol}. The potential of the interface charges is given by $\Psi_i - \Psi_{sol}$. This comes from a charge double layer at the liquid – insulator interface with the surface potential Ψ_i at the insulator side, and the potential drop Ψ_{sol} at the solution side. With this

$$V_{fb} = \phi_{sol} - \phi_s + \Psi_i - \Psi_{sol}. \tag{5.1}$$

Note that Ψ_{sol} is insensitive to ions. The detection of ions relies on the change of Ψ_i with ion concentration, which can be directly observed by a shift in V_{fb}. To ensure that ϕ_{sol} has a well defined potential, independent from the ion concentration it is essential to work with a reference electrode such as a calomel or an Ag/AgCl electrode.

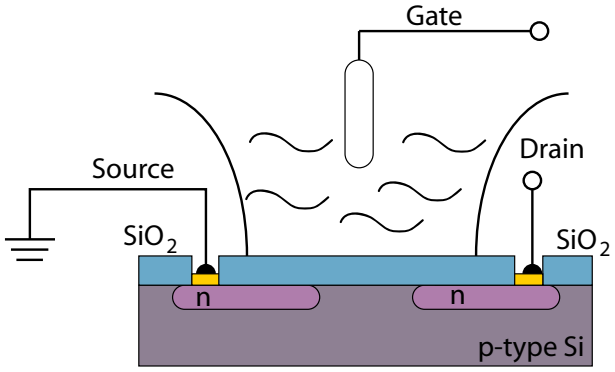


Figure 5.1: Scheme of a standard ISFET. P-type silicon with n-doped contacts regions. The metal gate is replaced by an electrolyte solution.

The gate dielectric is a critical part of the structure and defines the chemical sensitivity of the ISFET. Typical gate insulators such as SiO_2, Si_3N_4 or Al_2O_3 are sensitive to hydrogen ions so that they can be used as pH sensors. The gate oxide can be modified for the sensing of specific chemical or biological species. For example by immobilizing ligands at the gate oxide, bio–molecules can be specifically recognized. Figure 5.2(a) shows the example of an ISFET with protamine immobilized on the gate that specifically senses heparin [90]. Another type of sensors are Enzyme FETs (ENFET). Enzyme membranes are coated on the ion-sensitive gate for example to monitor specific enzymatic reactions. A standard example of such an ENFET is the penicillin sensor based on hydrolysis of penicillin by penicillinase as shown in Figure 5.2(b) [91]. For a review on ISFETs see [92, 93].

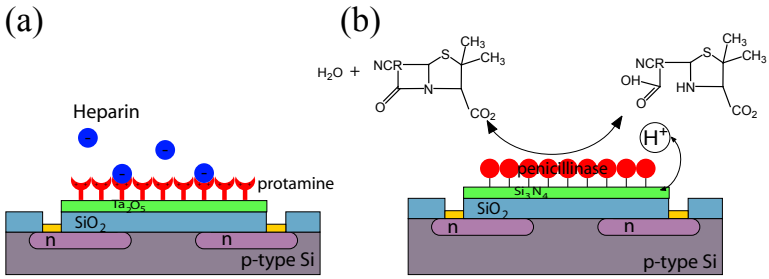


Figure 5.2: Scheme of modified ISFETs. (a) shows a heparin sensor with a ligand immobilized on the gate oxide. In (b) the immobilized penicillinase reduces penicillin and the hydrogen ions are sensed by the ISFET.

The fact that a bulk reference electrode is needed prevents ISFETs to be integrated into all solid state sensors. A way to circumvent this limitation is to measure differentially the ISFET signal and the liquid potential via an ion insensitive reference FET [94]. The challenge lies in constructing a FET which acts as ideal solid state reference electrode that is not sensitive to ion concentration, but still highly sensitive to changes in the liquid

potential. When aiming at *in vivo* sensing with ISFET technology one has to avoid applying the gate voltage via an electrolyte–gate: applying a gate voltage high enough to reach inversion in the FET channel can stimulate undesired responses in tissues. To avoid such effects, the gate voltage can be applied by a back–gate in case of a very thin semiconductor channel. This way the gate is isolated from electrolyte. Another main problem in ISFET technology is the stability of devices in liquid. Improvements in stability of chemically modified insulator – electrolyte interfaces and immobilized sensing functionalities are of high importance. A back–gate that helps avoiding to apply large electrolyte–gate voltages surely enhances stability.

Another approach for chemical FET sensing is to modulate the flat band voltage $V_{fb} = \phi_m - \phi_s$ of a MOSFET by changes in the work function of the gate metal. Redox active materials like iridium oxide or redox polymers can be used as gate materials to sense oxidative agents [95]. Palladium is well suited for hydrogen sensing [96].

5.1.2 Going for nano

Short after the first report on CNT FETs [14], their potential in sensing oxidizing or reducing gases has been realized and observed [97, 71]. These were followed by reports on electrochemical gating of CNTs in analogy to ISFET technology [98, 99]. This attracted high interest in adapting such devices for biosensors.

This high interest is driven by multiple arguments. Most obvious is the size compatibility between the sensing nanodevice and biological entities [100]. This is crucial when aiming at studies of microscopic mechanisms in biology at the level of a single organelle or even single molecules. Of main interest is the high sensitivity of the current in nanowires or nanotubes to adsorbed charges (see next paragraph). The fact that electrostatic interaction and charge transfer involved in most biological processes can be detected directly by an electronic device opens ways in merging biology and electronics. In addition it allows label free detection of bio–molecules via specific recognition by immobilized receptors [101, 102]. The small size

of the sensors results in small capacitances and therefore fast response. It permits to measure locally and allows integration into arrays of sensors and, further on, into complex Lab-On-Chip devices. This opens possibilities to correlate measurements in time and space for identical sensors and permits multiplex measurements on an array with differently functionalized sensors. The latter is important because reliable disease diagnosis often requires the identification of multiple molecular markers [103, 104]. Correlation measurements on an array of SiNWs have been used to monitor signal propagation in the axon of a neural cell [105].

Size dependance of NW sensors has been discussed looking at various aspects. In contrast to planar FET sensors, molecular charges on the surface of nanowire FETs can lead to accumulation or depletion of carriers in the "bulk" of a small diameter structure. The amount of induced charges by a change in surface potential is given by the semiconductor capacitance $dQ = C_s \cdot d\Psi_s$ (see Section 2.2). If the nanowire is small enough to reach uniform energy throughout its cross section, this capacitance reaches the quantum capacitance C_q. Therefore reducing the nanowire width enhances the response to a given change in potential at the sensitive oxide as reported experimentally and by simulations [106]. When designing sensing assays that make best use of the high potential sensitivity of NW and CNT FETs, one has to consider other size effects. Nanoscale sensors are not suited for the detection of minute concentrations of trace elements because of the small volume they are sensitive to. The response time of the sensor is limited by diffusion of analyte molecules to the sensor surface — assuming irreversible adsorption. The smaller the sensing surface, the smaller the chance of analyte molecules to diffuse to it. This might lead to a very slow sensor response [107]. Reversible adsorption gets increasingly important for small concentrations which limits sensitivity even more [108]. These statements are still under debate arguing that for lower dimensional sensors not only one dimensional diffusion to a planar surface has to be considered. Including this consideration, response times of low dimensional nanosensors scale much slower when decreasing concentration than of planar devices [109]. Experiments will have to show how all these effects combine to the effective sensitivity. Small concentrations, below 10 fM, of streptavidin [41] and PSA (prostate specific antigen) [104]

have been detected in low ionic buffer solutions by SiNW FETs. A big advantage of nanoscale devices is the fact that they can handle minute sample volumes and they are sensitive to a small amount of molecules. A response to as few as ~ 10 streptavidin molecules has been reported for biotin functionalized CNT FETs [110]. This suggests that single molecule detection can be envisioned with such devices. Sensitivity of nano-sensors to single (large) biological objects has been impressively demonstrated by realtime monitoring of individual viruses attaching and detaching on a SiNW FET [111].

Whenever nano FETs are used as transducers for specific molecular recognition or reaction the sensor has to be functionalized. In the case of SiNW FETs this can be done by covalent binding to the native SiO_2 layer or the freshly prepared Si sidewall. Covalent chemistry on CNTs severely affects their electronic properties [112] which is not acceptable for FET devices. Therefore, recently much effort has been dedicated in non covalent functionalization. Pyrene groups for example interact strongly with CNTs via π-stacking [113, 114] and can be used in linking molecules for further functionalization. This way glucose oxidase was immobilized and its enzymatic activity could be monitored [115]. Another approach is the adsorption of polymers such as polyethylene imine (PEI) and poly(ethylene glycol) (PEG) [110] or Tween [116] that can be further modified with specific receptor molecules. In a similar way ss-DNA has a high affinity to CNTs as described in Appendix C.3, which was used in a specific DNA sensing assay on CNT network FETs [117].

For a more detailed overview on nano FET based biosensing see [118] for SiNW FETs and [100] for CNT FETs. Although a multitude of impressive biosensing experiments with SiNW and CNT FETs has been reported interest in simple pH sensing by SiNW FETs is increasing [119, 41, 106]. On one hand pH sensing with surface groups of SiNWs is the most basic system to study sensing effects in more details, on the other hand one can expect industrial applications to come up soon. In case of CNT FETs simpler systems have been studied again in parallel to the above mentioned biosensing experiments. One example are theoretical and experimental studies of the adsorption of benzene derivatives on CNTs [120, 121, 122, 123]. Another example are most recent reports about electrolyte gating

and electrochemical aspects of CNT FETs in ionic solutions. Larrimore [124] reported that CNT FETs follow the electrostatic liquid potential and therefore act as reference electrodes. Minot [125] showed both, the effect of the electrostatic and of the chemical potential changes under unspecific adsorption of proteins. Heller showed experimentally [126] and theoretically [127] that the density of states in carbon nanotubes has to be considered when studying electrochemical aspects of CNT FETs.

For our studies on sensing presented in this chapter we focus on more detailed investigation in the electrolyte gating (Section 5.3) and pH sensing mechanism for SiNW FETs (Section 5.4). Then we show how sensitive CNT FETs are to various environmental effects (Section 5.5) and focus on stability issues on these devices (Section 5.6). A comparison of SiNW and CNT FET devices can be found in Chapter 6. But first the test setups used for measuring in liquid are described.

5.2 Setup for test in liquid

Most promising applications for nanoscale FET sensors are in the area of biosensing. For this it is essential to work in liquid. In this situation, any electrical contacts should be protected from the liquid. In addition one has to be able to control the electrostatic potential of the liquid. The setup has to enable adding analytes or exchanging liquids.

The electronic insulation is provided by device packaging as described in Section 3.3. The only parts in contact with liquids are the sensitive parts and the microscopic leads. For SiNW FETs the leads are covered by the top oxide and only the side walls are in touch with the liquid. This way leakage currents are below 10 pA at 10 mV bias in 1 M KCl solution. For CNT devices the metallic contacts are not protected, but as small bias voltages of 1 mV are used, leakage currents are about 1 pA for 10 mM NaCl.

Two different setups are used to bring the device in contact with liquids. In the first one the chip is placed upside down in a beaker as shown in Figure 5.3. A home made cover with a socket holds and contacts the

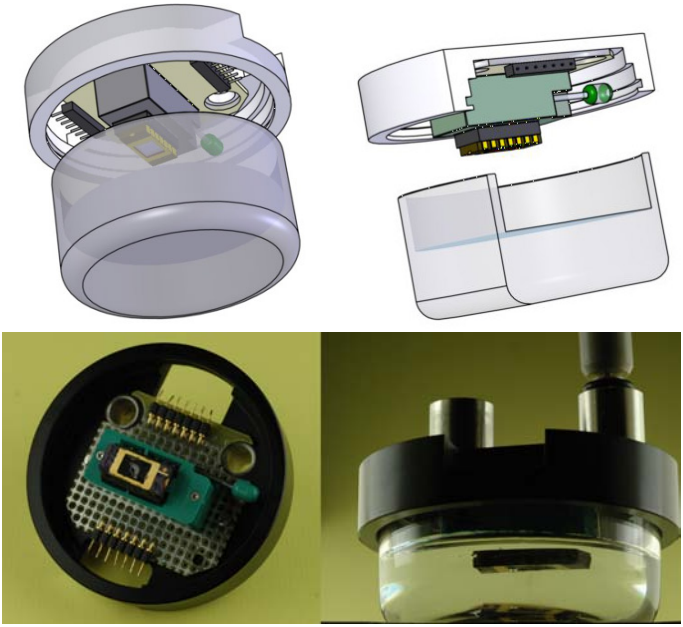


Figure 5.3: Schematics and photographs of the open liquid setup. The chip sits in a socket mounted at the cover of the glass beaker. The beaker is filled with liquid to a level that reaches the chip, but not the socket.

chip. The pins have to be protected by epoxy. Then only the protected part of the chip is in liquid and the socket is above. The liquid can be stirred by a magnet and heated by a hot plate. The opening of the cover allows access to a pipet and an electrode. For the second setup the chip sits upwards in the socket and a flow cell was mounted on the chip as shown in Figure 5.4. With a spring it can be pressed to the chip so that the o-rings act as a seal. Solutions can be pumped trough by a peristatic pump. A platinum wire, serving as an electrode, is mounted in the liquid cell. A silver wire is used as quasi-reference electrode and is mounted in the tubing connection.

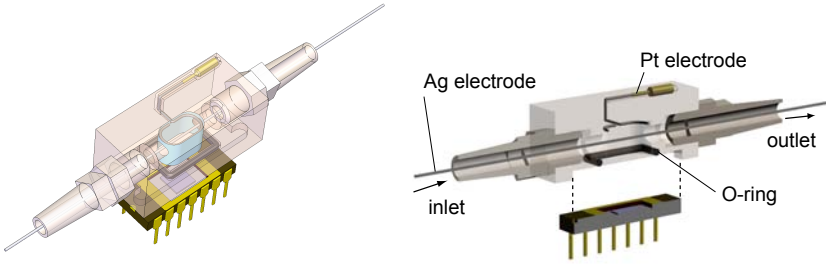


Figure 5.4: Schematics of the liquid cell. The chip is drawn with some distance to the o–ring for a better view. The cell is pressed on the chip which is sitting on a socket.

5.3 SiNW FETs in liquid

The behavior of SiNW FETs in an electrolyte solution is studied in this section. We start with the influence of the solution on the back–gate response and then describe electrolyte gating. Focus lies on the combination of the two. Stability issues are considered in Subsection 5.3.3.

5.3.1 Transfer characteristic in liquid environment

First we compare the behavior of nanowire FETs in air and in liquid environment. As in our design the nanowire is on top of the gate oxide it is exposed to the environment. When the sample is immersed in liquid the dielectric environment of the nanowire is changed dramatically. In Section 4.1.5 we saw that the electric field of the gate penetrates the nanowire from different directions. It penetrates the bottom, directly via the gate oxide, but as well the sidewalls via the nanowire surrounding. In presence of an electrolyte, the back–gate can couple to the solution capacitively via the back–gate oxide. This enhances the total gate capacitance as shown in Figure 5.5. The back–gate response of a SiNW FET is compared in air (black) and in 1 mM NaCl (red) in H_2O. On the p-side, the slope of the transfer characteristic in electrolyte is 5 times larger than in air. The inset shows the liquid potential monitored by a silver wire. For negative back–gate voltages it partially follows the gate voltage. This way the liquid potential acts as a parallel gate which can be accounted for as an increased effective gate coupling.

In the n-regime the transfer characteristic is the same in air and in liquid. The reason is that the liquid potential does not follow in this regime as seen from the inset. The nanowire seems to be slightly inverted for the small liquid potential which enables electron current in the case of inverted contacts. The potential of the liquid can be forced to be constant by inserting a grounded Pt electrode. In this case the conductance in the p-regime is completely suppressed. The reason is that the electrolyte potential couples stronger to the nanowire than the back–gate does. Therefore the nanowire stays depleted or slightly inverted for all back–gate voltages. These effects are studied in more details below.

5.3.2 Electrolyte gating

In presence of an electrolyte, the nanowire surface potential depends strongly on the potential of the electrolyte. This potential can be modulated via the platinum electrode. As this is a highly polarizable electrode

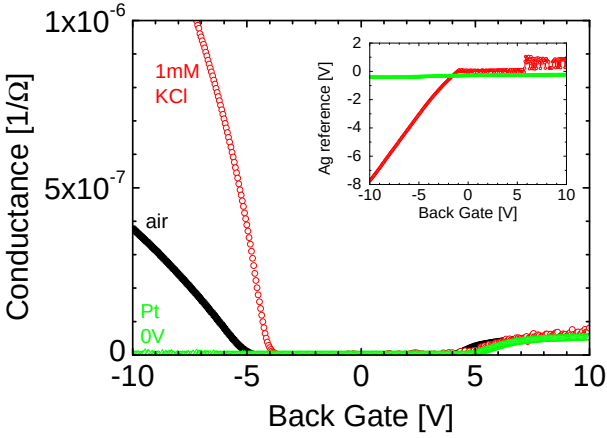


Figure 5.5: SiNW FET in air (■) and in 1 mM KCl without (◯) controlled liquid potential and with Pt electrode at $V_{pt} = 0\,\mathrm{V}$ (△). Inset shows the liquid potential monitored by a Ag wire with floating (◯) and grounded (△) Pt potential. $dG/dV_g = -8.3{\cdot}10^{-8}\,(\mathrm{V}\Omega)^{-1}$ in air and $-3.8 \cdot 10^{-7}\,(\mathrm{V}\Omega)^{-1}$ in KCl.

[128, 129] the liquid potential has to be monitored by a reference electrode. A calomel electrode was used in case of measurements in the beaker. In the closed liquid chamber, a silver wire was used as simple quasi - reference electrode. The nanowire is kept on zero potential (with a small ac modulation of 10 mV) via source and drain (see Figure 5.6(b)). The potential difference between the liquid and the grounded nanowire defines the electric field that gates the SiNW FET. This field between the liquid and the nanowire causes ions to accumulate around the nanowire as sketched in Figure 5.6(b) and it induces charge carriers in the nanowire. The ionic double layer charge couples strongly to the nanowire as it is separated by very thin native oxide only. For a simple estimation of the electrolyte–gate capacitance a model is used of a plane capacitor between the sidewall of the nanowire and the liquid in distance λ which is the Debye length given by

$$\lambda = \left(\frac{\varepsilon kT}{2 z_{ion}^2 e^2 c} \right)^{1/2}.$$

c is the ion concentration in m^{-3} and z_{ion} is the charge state of the ions. λ is of the order of 10 nm for a monovalent ion concentration of 1 mM. With this we get a double layer capacitance of

$$C'_{dl} \sim \frac{\varepsilon_{H_2O}\varepsilon_0}{\lambda} \sim 0.1 \frac{\mathrm{F}}{\mathrm{m}^2}. \tag{5.2}$$

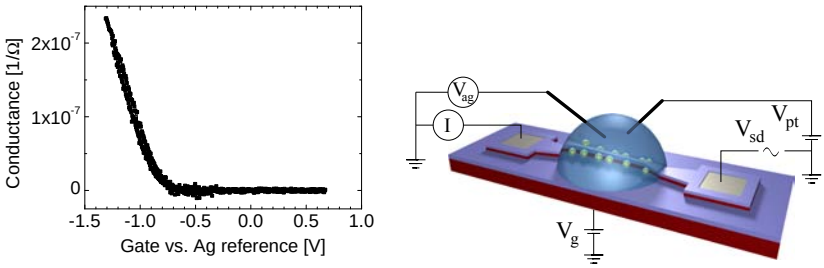
This capacitance is larger than the semiconductor capacitance C'_s of our nanowires. C'_s is estimated to be in the range

$$2 \cdot 10^{-3} \frac{\mathrm{F}}{\mathrm{m}^2} < C'_{d,nw} \leq C'_s \leq C'_{acc} \leq 2 \cdot 10^{-2} \frac{\mathrm{F}}{\mathrm{m}^2}$$

where $C'_{d,nw}$ is the depletion capacitance estimated in Section 4.1.5 and C'_{acc} is capacitance of the accumulation layer where $W_{acc} = 5\,\mathrm{nm}$ was chosen. This means that C'_s dominates the sensitivity in both regimes, accumulation and depletion.

The gating effect of such an electrolyte–gate is shown in Figure 5.6(a) where the conductance of a nanowire FET is plotted against the liquid

potential with a silver wire as reference in 1 mM KCl. In the linear region the conductance changes with $G \propto -4.9 \cdot 10^{-7} \cdot V_{ag}$. Compared with Figure 5.5 we see that the electrolyte–gate is 6 times more efficient than the back–gate in air. To verify with theory: $C'_{ox} \cdot 6 \simeq 3 \cdot 10^{-3}\,\mathrm{F/m^2}$ is in the range for C'_s given above. ($C'_{ox} \simeq 4.7 \cdot 10^{-4}\,\mathrm{F/m^2}$ is calculated in Section 4.1.5.)



(a) (b)

Figure 5.6: Conductance versus reference potential of SiNW FET in 1 mM KCl. The gate V_{pt} was applied to Pt wire, measured by an Ag wire (V_{ag}) as reference electrode as shown in the sketch. Same sample as in Figure 5.5.

To characterize the relation between the liquid potential and the applied gate potential we plot the Ag reference potential V_{ag} as function of the applied voltage V_{pt} on the platinum electrode for various back–gate voltages V_g (see Figure 5.7). The liquid potential follows V_{pt} with a shift of $\sim -150\,\mathrm{mV}$ for small back–gate voltages. The shift deviates by another $-160\,\mathrm{mV}$ for $V_g = -6\,\mathrm{V}$ and by $70\,\mathrm{mV}$ for $V_g = 6\,\mathrm{V}$. The slope is $dV_{ag}/dV_{pt} = 0.985 \ldots 0.995$.

Our geometry allows to apply a back–gate voltage and an electrolyte–gate simultaneously. The electrolyte–gate influences only the nanowire and parts of the leads (sketched in Figure 5.6(b)) as everything else is sealed with epoxy. On top of the device there is a SiO_2 layer so the electrolyte–gate primarily acts from the sidewalls. Since the nanowire is

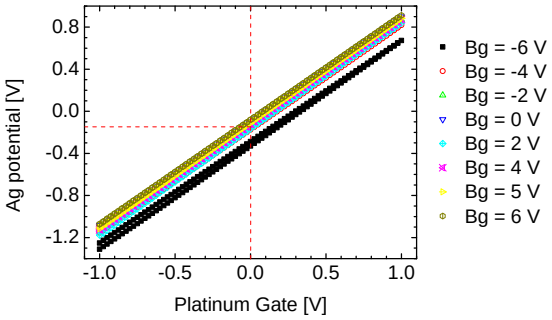


Figure 5.7: Measured potential of an Ag electrode vs. applied Pt potential for various back–gate voltages in 1 mM KCl. Ground is defined by source and drain of a SiNW. Horizontal dashed line: $V_{ag} = -150\,\mathrm{mV}$.

smaller than the depletion length W_d, not only the side wall surfaces, but the bulk NW is influenced. The leads are much wider than the nanowire, therefore they are only affected at the side wall surfaces. The electrolyte couples much stronger to the nanowire than the back–gate as seen in the previous paragraph. The potential of the nanowire is therefore predominantly controlled by V_{pt}. The back–gate on the other hand couples to the entire device structure. Its influence is overpowered by the electrolyte–gate at the nanowire only. We can gate the contacts with leads and the nanowire independently by back–gate and electrolyte–gate respectively. An overview of the effects of the back–gate V_g and the electrolyte platinum gate V_{pt} is shown in Figure 5.8. The conductance of the SiNW FET is plotted in colors against the back–gate voltage V_g and the electrolyte–gate voltage applied to the platinum electrode V_{pt}. In the lower left corner where V_g and V_{pt} are both negative, the contacts and the nanowire are in accumulation regime (p). A current can be carried by the induced holes. In the upper right corner both, contacts and nanowire are in inversion regime (n), so that the SiNW FET is in electron conductance

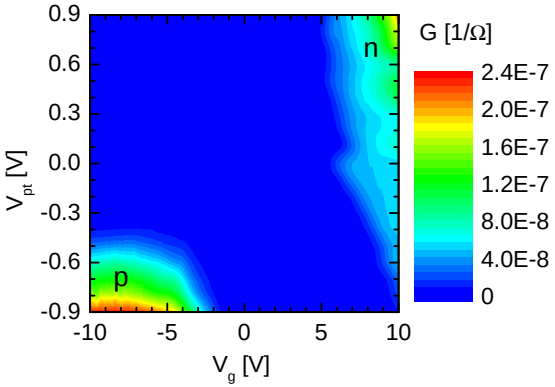


Figure 5.8: SiNW FET in 1 mM KCl electrolyte (pH 7). Conductance vs. back–gate V_g and electrolyte–gate V_{pt}. Same sample as in Figure 5.5.

regime. In the other two corners of the color plot opposite charges are induced in contacts and nanowire. In the upper left corner the contacts are driven to accumulation by the back–gate and the nanowire is inverted by the electrolyte–gate. In this p-n-p configuration, the current is blocked by two p-n junctions. From analogous argumentation, we conclude to a n-p-n configuration in the lower right corner. In the central part, the conductance is suppressed because the nanowire, the contacts or even both are depleted. The situation is not symmetric with respect to 0 V because of different threshold voltages in n and p regime for back–gate and electrolyte–gate. To compare the efficiency of the electrolyte–gate and the back–gate one can measure the slope of equipotential lines in the contour plot of Figure 5.8. One has to chose a region where both gates are in linear region. On the p-side the slope of $\triangle V_g/\triangle V_{pt} = 5.5$. On the n-side it is $\triangle V_g/\triangle V_{pt} \simeq 5$ for small V_{pt} and $\triangle V_g/\triangle V_{pt} \simeq 2$ for high V_{pt}. In this region, the contacts seem to dominate. For a more detailed study we look at conductance traces in the color plot at fixed V_g or V_{pt}.

Lets first consider the electrolyte–gate response for fixed back–gate volt-

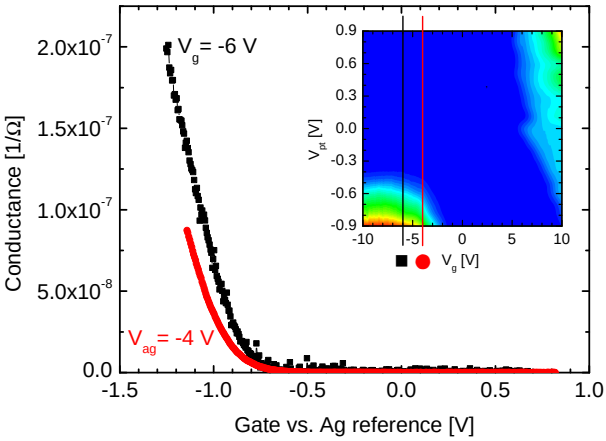


Figure 5.9: Accumulation regime: Conductance vs. liquid potential (Ag reference) at fixed V_g. This corresponds to vertical traces indicated in the color plot. The x axes is scaled to the Ag potential. 1 mM KCl.

ages. This corresponds to the situation of a MOSFET with fixed contact doping. We look at the situation of p-type contacts induced by a negative back–gate voltage. In Figure 5.9 the conductance of a SiNW FET and the liquid potential were measured simultaneously while the potential of a Pt electrode was swept. The conductance is plotted versus the potential of the reference electrode (Ag wire). For back–gate voltages of $V_g = -4\,\mathrm{V}$ and $V_g = -6\,\mathrm{V}$ the contacts are in p-regime and highly transparent. Conductance is suppressed for positive electrolyte–gate voltages V_{ag} and enhanced for negative V_{ag}. For both back–gate voltages $V_g = -4\,\mathrm{V}$ and $V_g = -6\,\mathrm{V}$ the contact regions and leads are more conductive than the wire and therefore there is only a small difference. The threshold voltage is very similar in both cases ($V_{th} = -0.88\,\mathrm{V}$ for $V_g = -4\,\mathrm{V}$ and $V_{th} = -0.82\,\mathrm{V}$ for $V_g = -6\,\mathrm{V}$) and the transconductance dG/dV_{ag} is slightly higher for more negative V_g ($dG/dV_{ag} = -4.1 \cdot 10^{-7}\,(\Omega\mathrm{V})^{-1}$ and $dG/dV_{ag} = -4.9 \cdot 10^{-7}\,(\Omega\mathrm{V})^{-1}$ for $V_g = -4\,\mathrm{V}$ and $V_g = -6\,\mathrm{V}$ respectively). This can be explained by a higher conductance of the leads if they are deeper in accumulation. The main difference between the two back–gate voltages is that the liquid potential is shifted by 160 mV. The fact that the back–gate has a minor effect below $-4\,\mathrm{V}$ can be seen nicely in the lower left corner of Figure 5.8 and in conductance traces for fixed V_{pt} shown in Figure 5.10. The contacts are highly transparent and the current is limited by the nanowire where the potential is controlled by the electrolyte–gate. With all this we see that truly the nanowire channel is the current limiting factor in this region.

In inversion mode, for positive V_g and V_{ag}, the situation is similar, but we cannot see any saturation as shown in Figure 5.11. But as we can see in the color plot (inset), the inversion side is cut off by the measurement window in the linear increasing region. Nothing speaks against a possible saturation at higher voltages. Note that in air, the back–gate response in the n-regime for the same device saturates at about $5.2 \cdot 10^{-8}\,\Omega^{-1}$ just as it does for $V_{pt} \leq 0\,\mathrm{V}$ (dashed line). If the nanowire is driven into inversion by an electrolyte–gate ($V_{pt} > 0\,\mathrm{V}$) this saturation is lifted. Therefore we conclude that the saturation has to come from the nanowire rather than from the contacts. In air the back–gate obviously cannot drive the nanowire far into inversion. Reminding the effect of the top oxide on the

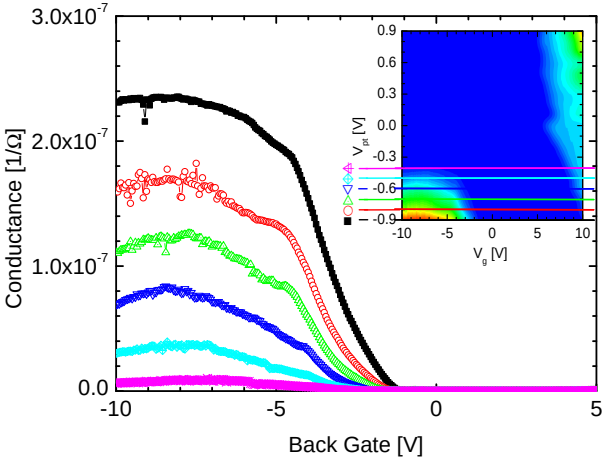


Figure 5.10: Accumulation regime: Conductance at fixed liquid potential and and varying back–gate. This corresponds to the traces indicated in the inset for $V_{pt} = -0.9, -0.8, -0.7, -0.5, -0.4$ V. 1 mM KCl.

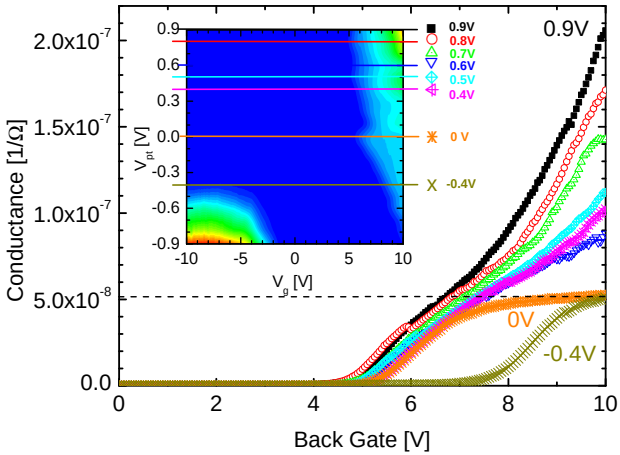


Figure 5.11: Inversion regime: Conductance vs. back–gate at fixed liquid potential. These are the traces for $V_{pt} = 0.9$, 0.8, 0.7, 0.6, 0.5, 0.4, 0 and $-0.4\,\mathrm{V}$ as indicated in the inset. Horizontal dashed line: $G = 5.2 \cdot 10^{-8}\,\Omega^{-1}$. 1 mM KCl.

saturation (see Figure 4.13), we conclude that the top oxide pins the energy level of the nanowire at its top side and avoids full inversion. Whereas the back–gate cannot overcome this pinning, the coupling electrolyte–gate is strong enough so that the pinning can only dominate in a small gate voltage window.

In summary, this section shows the high efficiency of the electrolyte–gate coupling. It is 5–6 times higher than the coupling of the back–gate. The electrostatic potential of the liquid can be controlled by a Pt electrode. The back–gate couples weakly to the liquid potential. This cannot be neglected, but the effective liquid potential has to be monitored by a reference electrode. The combination of back–gate and electrolyte–gate permits control of the charge carrier density of both, the nanowire and the contact region.

5.3.3 Stability of SiNW FETs liquid setup

To be confident about the reliability of the above explained measurements, fluctuations over long times have to be controlled. Stability issues arise rather from the not optimized measurements setup as from the SiNW FET devices. This can be seen by the comparison of the two liquid setups introduced in Section 5.2. In both cases the conductance of a SiNW was monitored overnight in 1 mM NaCl while the back–gate was set to a fixed value where the device is most sensitive. In case of the closed chamber the liquid was under constant flow of 1 ml/min. As one can see from Figure 5.12, the conductance G varies dramatically in an initial time which is in the range of 1 h in the open chamber and 5 min in the closed one. Then in case of the closed chamber it fluctuates around a value that decays by around 1 % per hour. These fluctuations can be reduced by stoping the flow. In case of the less controlled, open chamber G fluctuates by more than one order of magnitude. The reason for such drastic changes is not clear. An obvious reason would be the uptake of oxygen from air in case of the open chamber. This was tested by bubbling the liquid with N_2 and O_2 alternatively. The gases increase fluctuations as seen in Figure 5.13. But the effect of oxygen and nitrogen cannot be clearly distinguished.

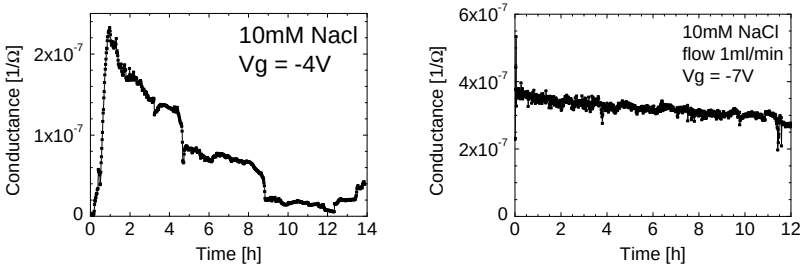


Figure 5.12: Fluctuation in open liquid (a) and in closed chamber (b).

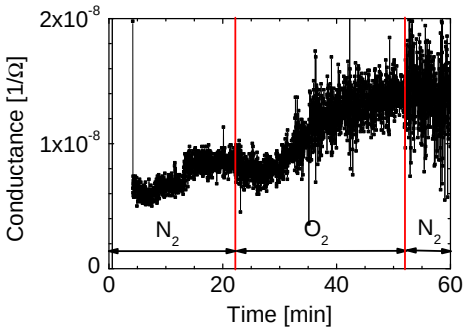


Figure 5.13: Effect of N_2 and O_2 bubbling in 1 mM NaCl solution on SiNW FET.

The degradation of the SiNW FETs is small. They could be used for for more than 200 experiments without degradation problems. As an example we show the transfer characteristic of a SiNW FET before and after more than 100 experiments in air and liquid during 6 weeks in Figure 5.14. One can see some changes in accumulation mode which is most sensitive to surface effects, but none in inversion. This shows that only the stability of the sensing nanowire surface has to be addressed when optimizing long term stability.

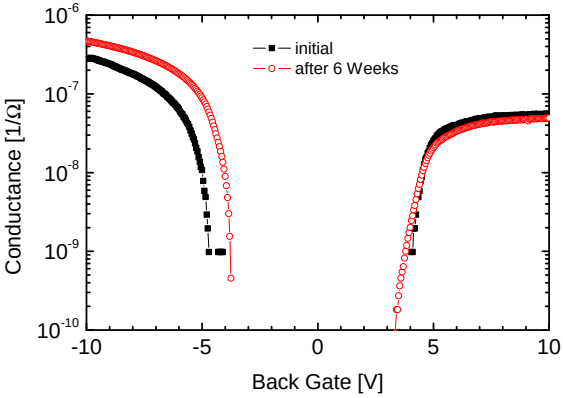


Figure 5.14: Transfer characteristics of a SiNW before and after more than 100 experiments in air and liquid, including high bias and electrolyte–gate experiments.

The devices respond to many environmental effects. A closed and well controlled test setup is therefore crucial. For further control of the setup the liquid potential and the temperature have to be stabilized. In addition the oxygen content in aqueous solutions has to be controlled which is done in most of our experiments by bubbling N_2 through the liquid for 2 h before and during measurements. To be able to measure in a less strictly controlled environment, differential measurements with two

differently functionalized nanowire FETs are suggested.

5.3.4 Summary

In conclusion, we see that SiNW FETs are very stable in liquid environment. Without any particular surface treatment, they can be used for months. In our devices the gate efficiency of the electrolyte–gate in 1 mM KCl is about 5–6 times higher than that of the back–gate. This is shown by two independent experiments: the comparison of back–gate response in air to the response in liquid, and the combination of back–gate and electrolyte–gate.

By combining back–gate with electrolyte–gate, the device can be tuned in regions where the nanowire channel is current–limiting and in regions where the contact regions are current limiting. Most sensing experiments on SiNW FETs reported in literature are performed only with a back–gate control, without electrolyte–gate [38, 41]. From our studies one can learn that one has to be careful when measuring in an aqueous environment with back–gate alone. The back–gate has an uncontrolled effect on the potential of the liquid. For well defined sensing experiments a controlled liquid potential is mandatory which is possible by the technique of combining back–gate with electrolyte–gate. Studies of electrolyte solutions with varying pH value using this technique are presented in the next section.

5.4 pH sensitivity of SiNW FETs

Only few reports address the pH sensitivity of SiNW FETs [38, 41, 119]. All three reports measure the conductance at a fixed gate voltage while the pH value of the liquid is changed. While the basic idea of all the reports is the same, the detailed outcome of all these experiments is still controversial. The surface charge of a SiO_2 surface and an amino propyl triethoxy silane (APTES) functionalized surface increases for decreasing

pH value. The reason is that -SiOH and -NH_2 end groups can be protonized or deprotonized by changing the pH value as shown in Figure 5.15. This charge on top of the surface acts as an additional gate. In standard ISFET sensing the gate voltage is applied via an electrolyte–gate. In Section 5.1.1 we saw that in this case the flat band voltage is given by (Equation 5.1)

$$V_{fb} = \phi_{sol} - \phi_s + \Psi_i - \Psi_{sol}. \tag{5.3}$$

If a potential is applied to the electrolyte–gate, the gate voltage above on-set is given by

$$V_{ag} - V_{fb} = V_{ag} - \phi_{sol} + \phi_s - \Psi_i + \Psi_{sol}$$

Ψ_i depends on the ratio of protonized to deprotonized sites whereas $\phi_{sol} - \phi_s$ and Ψ_{sol} should not be affected. When measuring the conductance at a fixed back–gate value and not controlling the liquid potential, it is not possible to know if changes in the effective gate potential come form Ψ_i or from another term. For this reason we study the response of the device conductance to back–gate and electrolyte–gate for different pH values.

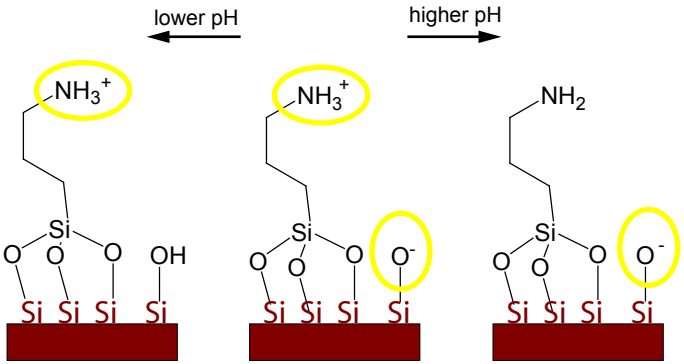


Figure 5.15: Sketch of pH dependence of surface charge of an APTES coated SiO_2 surface.

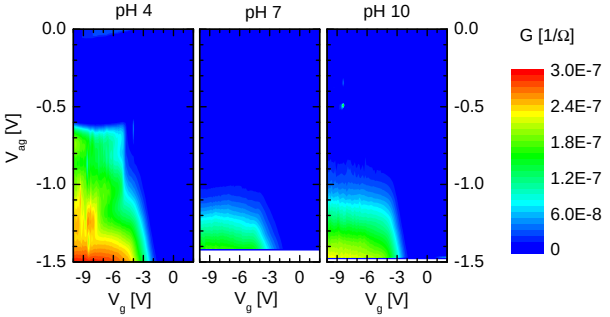


Figure 5.16: SiNW FET (no APTES): Conductance in color as function of back–gate V_g and liquid potential V_{ag} for pH 4, 7 and 10. Electrolyte: 1 mM KCl.

In Figure 5.16 the conductance of a SiNW is plotted as function of V_g and the liquid potential V_{ag}. The liquid potential was measured with a silver wire while applying a gate potential via the Pt electrode. For high negative gate voltages V_g and V_{ag} the device is in accumulation. When driving the liquid potential V_{ag} from 0 V to −1.6 V at constant back–gate of $V_g = -10\,V$ the conductance first suppressed and at an onset voltage V_0 it starts to rise. The most pronounced effect when comparing the same measurements for different pH values is a shift in the onset voltage V_0 for V_{ag}. It is in the same range for pH 10 and pH 7, but increases for pH 4. Transfer curves in air after each measurement confirm that the observed effect does not come from drift, but is a real sensing effect (see Appendix Figure B.2). The point of zero charge (pzc) at the SiO_2 surface is at pH 3 [130, 131]. Therefore we expect the surface charge of SiO_2 to be sensitive for pH changes in low range, but much less for high pH, just as we see in Figure 5.16. The high conductance region in these graphs is the accumulation regime and its onset voltage corresponds to the flat band voltage V_{fb}. Higher values of V_{fb} as it is the case for pH 4 means

more positive insulator potential Ψ_i (see Equation 5.3), which means more negative surface charges. (Note: an alternative way to see this is that an increase in V_{fb} means that the wire is more p-doped. The mirror charge on the insulator surface is negative). This is in contrast to what we expect for lower pH, which corresponds to high concentration of hydrogen ions. Further investigations have to be done to explain this effect.

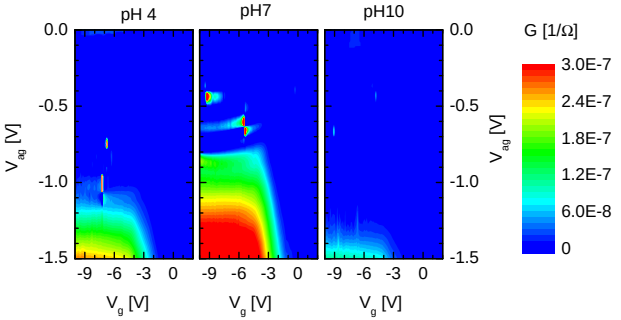


Figure 5.17: SiNW FET with APTES: Conductance in color as function of back–gate V_g and liquid potential V_{ag} for pH 4, 7 and 10, 1 mM KCl.

The same measurement for an APTES functionalized SiNW FET is shown in Figure 5.17 (for APTES coating: see Appendix C.6). The pH value for point of zero charge (pzc) is expected to be around 7, as both, APTES (with pzc pH 11) and SiO_2 (pzc pH 3), can contribute [130]. The shift to more negative values of V_{fb} for low pH 4 corresponds to what we would expect for positive charges at the SiO_2 – liquid interface. The shift to more negative values of V_{fb} for pH 10 is in opposite direction as it was without APTES. Note that with and without APTES, the flat band voltage for the expected point of zero charge is similar. The slope dG/dV_{ag} is very high for these two cases whereas it is smaller for lower V_{fb} values.

These first test measurements of pH variation by an electrolyte–gated SiNW FET show a very pronounced shift in onset voltage V_0 of the reference potential V_{ag} for back–gate values in strong accumulation $V_g < -4\,\mathrm{V}$. Further investigations have to reveal the details of the responsible effects. When sweeping the back–gate V_g at a liquid potential $V_{ag} \neq V_0$ the onset of the back–gate response is independent of the pH value. But the conductance saturation for high back–gate voltages does vary (see Figures 5.16 or B.3). It follows that the standard readout scheme for ISFETs of adjusting the gate to source potential to be near the threshold voltage cannot be directly transferred to back gated devices. In previous reports on pH sensing only one gate was used [38, 41]. This is not a reliable experiment as changes in liquid potential and pH value cannot be separated, as shown in Section 5.3.2. In contrast the concept of applying back–gate and electrolyte–gate enables finding a measuring window where pH variations have a strong effect on the SiNW FET.

5.5 Sensitivity of CNT FETs

The fact that carbon nanotube FETs (CNT FETs) are very sensitive to their environment has been observed and described by many groups [71, 97, 98]. Various effects can alter the electronic properties of nanotubes. Here we study these effects by three different types of systems as shown in Figure 5.18: Molecules adsorbed on the nanotube sidewall, ionic charges in liquid environment and dipolar molecules leading to an effective gating. High sensitivity is found in all three experiments as described in Sections 5.5.1-5.5.3. Difficulties in sensing assays with CNT FETs are pointed out in Section 5.6.

5.5.1 Sensitivity of CNT FETs to adsorbates

To show the high sensitivity of CNT FETs to adsorbates the effect of different benzene derivatives adsorbed on a CNT channel are shown in Figure 5.19. The adsorbates in use were aniline, phenol anisole, toluene, chlorbenzene and nitrobenzene. The chemical formulas of these compounds

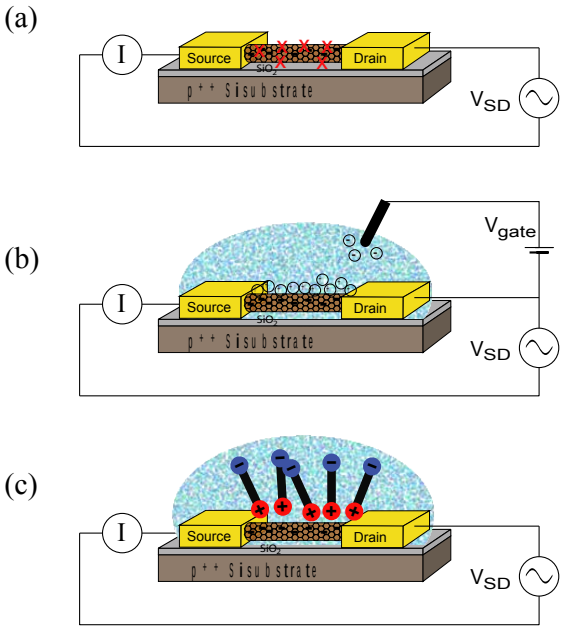


Figure 5.18: CNT FET sensing schemes: (a) molecules adsorbed on the CNT surface, (b) electrolyte gating, (c) gating via orientation of dipolar molecules.

from top do bottom are shown on the right of Figure 5.19. The common phenyl ring is responsible for the sticking of the molecules on the tube. The side groups differ in their ability of donating or withdrawing electrons. The affinity of benzene derivatives to nanotubes by $\pi - \pi$ interaction has been calculated to have a binding energy of 0.2 eV [122]. They were all solved in cyclohexane by 0.2 M. For each measurement the CNT FET was first washed in chloroform and cyclohexane, then incubated in the desired solution and blown dry by nitrogen flux. The back–gate response was recorded in ambient environment. Comparing the different curves of Figure 5.19 we observe that the most important effect is that the back–gate response curves are shifted in respect to each other. Such a shift can come from charge transfer between adsorbates and the carbon nanotube. Most pronounced is the effect of aniline. This is a strongly electron donating molecule. Therefore the intrinsic p-doping of the nanotube is partially compensated. This results in a shift to the left by about two volts.

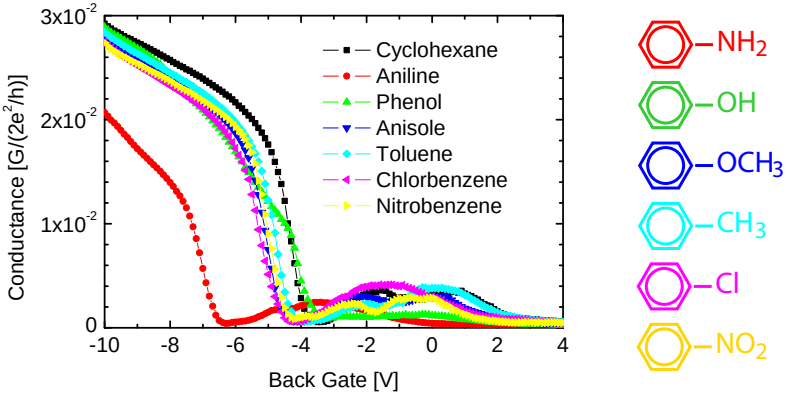


Figure 5.19: CNT FET with different benzene derivatives adsorbed.

Note that this is not a doping in terms of electrons injected into the nanotube. It is rather an electrostatic interaction between the molecules and the electronic π-system of the nanotube. This effect has also been

observed by others [120] and has been studied theoretically [121, 122, 132, 123]. Simulations show only minor charge transfer to the CNT, but introduction of scattering centers is predicted [121]. This would reduce the hole mobility and thus the transconductance dG/dV_g which we don't observe. Our findings rather support the experimental observation of Star [120].

We see that carbon nanotube FETs are very sensitive to the chemical properties of the environment the nanotube channel is exposed to. But repeated experiments with benzene derivatives ended in various outcome. One of the main reasons for our bad reproducibility is that the resistance of nanotube - metal contacts differs from device to device and can change over time or when exposed to liquid. For this reason nanotube - metal contacts are studied in more details in Section 5.6.1.

5.5.2 Electrolyte gating

Electrolyte gating is a concept that comes from the ISFET technology [92]. In the context of nanotube transistors it has been introduced by Krüger et al. [98]. Carbon nanotube FETs are immersed in an electrolyte solution and a gate voltage is applied by a metal gate electrode. Such an electrode can be implemented by a platinum wire or by a lithographically patterned on chip electrode. As carbon nanotubes are not surrounded by any oxide, the ions from solution are in intimate contact to the tube. The gate coupling becomes extremely efficient. To give an estimation of the gate capacitance of such an electrolyte–gate we compare it to a cylindrical capacitor.

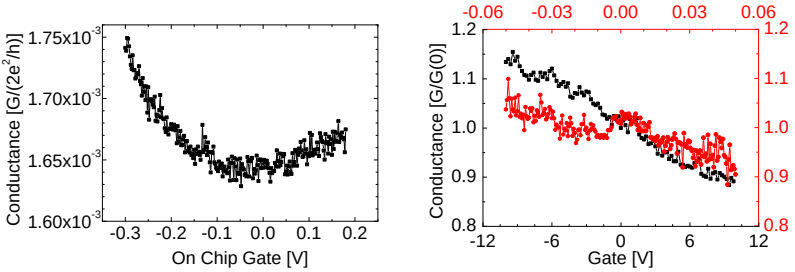
$$C^\star = \frac{C}{L} = \frac{2\pi\varepsilon_0\varepsilon_{H_20}}{\ln\left(\frac{r_{NT}+d}{r_{NT}}\right)}$$

The dielectric constant of water is $\varepsilon_{H_20} \approx 80$. As distance d between the capacitor plates we use the Debye length λ of the electrolyte solution

$$\lambda = \left(\frac{\varepsilon kT}{2z_{ion}^2 e^2 c}\right)^{1/2}$$

where c is the ion concentration in m-3 and z_{ino} is the charge state of the ions. For a monovalent ion concentration of 100 mM, $\lambda \sim 1$ nm. Assuming a nanotube radius of 1 nm leads to an electrolyte–gate capacitance of 6 nF/m.

The capacitance of the system is governed by the quantum capacitance which is much smaller ($C_{NT} \sim 320$ pF/m from Equation 2.14) than the electrolyte double layer capacitance. From Equation 2.13 follows directly that $dE_f = edV_g$ [98].



(a) (b)

Figure 5.20: Electrolyte gating of CNT bundle FETs. (a): 100 mM NaCl, conductance in the off state of the CNT bundle. (b): back–gate (■) in air on bottom scale and electrolyte–gate (●) in TE buffer on top scale. Conductance is normalized by its value at $V_g = 0$. Device with bundles of CNTs.

The high efficiency of the electrolyte–gate can be seen in Figure 5.20. In Figure (a) the gate potential is applied via 100 mM NaCl by an on chip electrode of Pd in this case. The CNT bundle device is in the off state at $V_g = -0.04$ V and can be tuned from p to n region by a total gate range of 0.5 V. With back–gate the n region is never reached for our channel limited nanotube FETs. For a more quantitative investigation of the gate efficiency we compare measurements in air gated by back–gate with measurements in TE buffer (10 mM Tris, 1 mM EDTA) gated by an on chip electrode. They are shown in Figure 5.20(b) for a device of

nanotube bundles. Note that the scale for the applied back–gate is 200 times larger than the scale for the electrolyte scale. Therefore we can estimate that the electrolyte–gate is nearly 200 times more efficient than the back–gate of 400 nm SiO_2. Similar enhancement has been observed for MWCNTs for electrolyte–gate [133].

When a nanotube FET is in an electrolyte environment without electrolyte gating, but the back–gate is swept, the gate efficiency is enhanced as shown in Figure 5.21. To explain this we have to consider that the back–gate can capacitively couple to the electrolyte. Therefore the electrolyte partially follows the potential of the back–gate and efficiently acts on the nanotube.

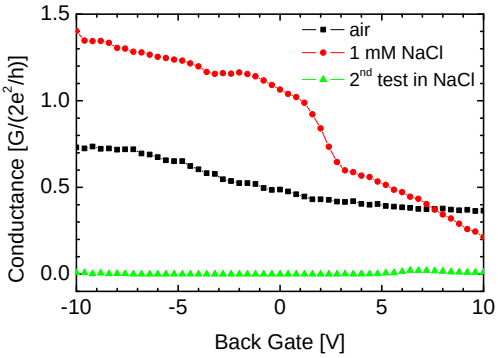
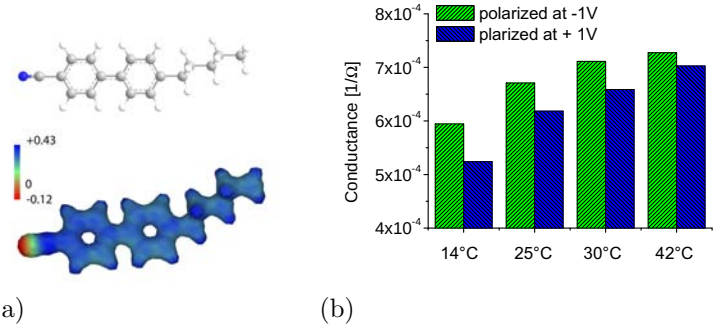


Figure 5.21: Back–gate transfer characteristics of a CNT FET device (nanotube bundle) in air (■) and immersed in 1 mM NaCl (● and ▲ short after). Enhancement by factor ~ 3.

Whenever measuring in aqueous electrolytes nanotube transistors are destroyed within minutes. This can be seen in the example shown in Figure 5.21 where after measuring a first time (red circles) the conductance is lost (green triangles). The reason for this is not so clear as carbon nanotubes are chemically very inert and no chemical interaction are expected. The contact region might be most delicate as described in Section 5.6.1.

5.5.3 Gating by dipole orientation

In the above examples of Section 5.5.2, ionic solutions are used to build up an electrostatic potential gating the nanotube. Non charged molecules with a high dipole moment can act the same way. To show this a liquid crystal solution is placed on a nanotube FET. We used pentyl cyanobiphenyl (5CB). The molecular structure of 5CB is shown in Figure 5.22 (a). It has a very polar cyano group on one side and a very non polar C-5 chain at the other end. The total dipole moment is 3.8 D ($\simeq 1.3 \cdot 10^{-29}$ Cm). This value was calculated numerically by HyperChem. By the two phenyl rings in the center they tend to align at low temperature. These dipolar molecules can be aligned by exposing them to an electric field. At lower temperature they tend to keep this orientation when the field is released, at higher temperatures they reorient randomly.



(a) (b)

Figure 5.22: Gate effect of oriented dipoles on a CNT bundle FET. (a) shows the structure of 5CB and the charge distribution (isosurface of charge distribution, color coding of electrostatic potential, calculated by HyperChem). (b) shows the conductance after orienting the dipolar molecule 5CB with -1 V (green) and $+1$ V (blue) for different temperatures. On chip gate $V_g = -0.6$ V for measurements (find details Figure B.4).

A solution of 5CB was placed on a CNT FET. The molecules were ori-

ented by a potential of $\pm 1\,\mathrm{V}$ via an on chip electrode. Then the on chip gate was ramped to the the measuring value of $-0.6\,\mathrm{V}$. In Figure 5.22(a) the conductance is plotted as measured after $-1\,\mathrm{V}$ orientation (green) and after $+1\,\mathrm{V}$ orientation (blue) for various temperatures. One can see that for lower temperatures there is a larger difference between the conductance for oppositely oriented dipole moments of the molecules. When the temperature is increased this difference decreases as one expects for less strongly oriented liquid crystals. Note that this experiment is done on a device with nanotube bundles as channel - this means that metallic tubes are in parallel that cannot be gated. The fact that the gating effect of oppositely oriented dipolar molecules is still pronounced shows the high local sensitivity of nanotube FETs.

The three reported sensing experiments on CNT FETs show very high sensitivity to

- charge transfer from molecules to the CNT,
- an electric field of nearby ions and
- an electric field of oriented dipolar molecules.

In addition the experiments show that the stability of CNT FETs in liquid environment has to be addressed.

5.6 Stability of CNT FETs

In the previous Section we have seen that in CNT FETs we can use two effects for sensing: First, the effect of electrostatic interaction between nanotube and molecules at its surface. This was shown by the interaction with the net charge of ions or with the charge distribution of the molecules in case of benzene derivatives. Secondly, the gate coupling can be modified using electrolyte gating. Other influences on the nanotube have to be ruled out. Figure 5.23 sketches the effects of adsorbates and gate coupling (marked in blue) and undesired effects marked in red. It is known that

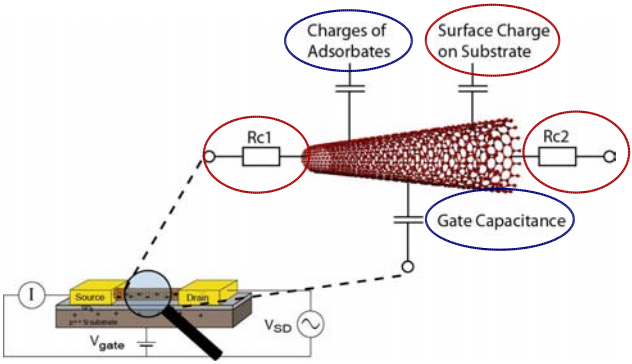


Figure 5.23: Environmental effect on CNT FETs. Effects described in the previous section in blue, further effects discussed below in red.

environmental effects can affect the contact resistance [20] and the silicon oxide substrate [49]. Both effects lead to unwanted changes in nanotube conductance and have to be controlled. In the following subsections these issues are addressed.

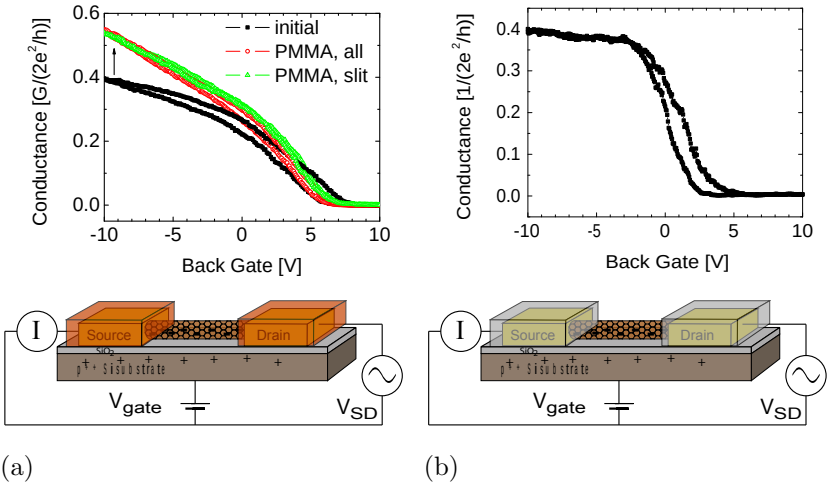
5.6.1 Carbon Nanotube - Metal contacts

The contact between the metals and the carbon nanotube can be influenced by molecules in its direct vicinity [134, 135, 136]. Therefore we have to protect the contact region. We discuss here three approaches.

PMMA contact passivation

Simple contact protection can be carried out by PMMA. The polymer is spun on the device. Between the metal contacts a small slit is opened

by e-beam lithography. Figure 5.24(a) shows an example of a PMMA passivated device. One finds a reduction in hysteresis and increase in on–current after the device is covered with PMMA. The increase in on–current could come from the increased dielectric constant of PMMA compared to air. The decrease in hysteresis is attributed to a reduction of the water layer around the nanotube (See Section 4.2.4 and [86, 87]). Opening a slit between the contacts does not influence the behavior very much. In some cases an increase of hysteresis was observed, but not systematically. Note that it is not evident [64, 65] that writing with e-beam at 35 kV on the nanotube does not affect the transport properties.



(a) (b)

Figure 5.24: Transfer characteristics of CNT FET with PMMA covered contacts (a) and SiO_2 covered contacts (b).

Ions and gas molecules can diffuse through PMMA and therefore it is not the best protecting layer. Nanotube contacts were as easily destroyed as without PMMA. But from the observation of Figure 5.24(a) we see that devices with covered contacts show even better performance.

SiO_2 contact passivation

The contact regions were covered by SiO_2. Figure 5.24(b) shows the transfer characteristics for such a device. We find that the device characteristics are not degraded, in particular the hysteresis is small. A strong pronounced hysteresis due to trap states at the new oxide–nanotube interface could be expected, but was not observed. Two fabrication approaches were tested. First on a PMMA covered device an area that is slightly larger than the contact metals is defined and opened by e-beam lithography. Then the device is annealed in vacuum to remove adsorbed water molecules. SiO_2 is deposited by evaporation as described in Appendix C.5. The problem of this approach is that the lift-off of SiO_2 is difficult and the gap between the electrodes is designed very small. A second approach consists in covering the entire sample with SiO_2 by evaporation. A small slit is then opened in a PMMA mask on top by e-beam lithography and a hole etched in the top oxide by buffered HF. The problematic of this approach is that PMMA is a bad mask for HF etching. Holes were much wider than designed by lithography and extended the metal contact separation.

Alkane thiol monolayer on contact metal

With the idea of protecting the metal contacts via a simple procedure, alkane thiols were assembled on the metal contacts. Characterizing such devices lead to the interesting observation suggesting that carbon nanotube parts below palladium contacts cannot carry any current. As consequence the current is forced in the nanotube at the metal edge.

To assemble an dodecane monolayer on the contacts, devices were incubated in 1 mM C_{12}-SH in ethanol for several hours and then washed twice in pure ethanol for 15 min. With such a C_{12} thiol monolayer SWNTs don't carry any current at all (resistance $\gg 100\,\mathrm{M\Omega}$), as the example in Figure 5.25(a) shows. The conductance cannot be restored by washing in pure ethanol overnight or by annealing for 3 hours at 600° C in vacuum of $2 \cdot 10^{-6}$ mbar. There are two possible explanations for the loss of conductance:

1. The nanotube is destroyed by a chemical reaction.

2. The contact between the metal and the nanotube is suppressed.

It is known that thiols do no react with carbon nanotubes [137, 70, 138]. And neither alkane chains nor strongly electron withdrawing molecular groups can totally suppress the conductance as my experiments in Sections 5.5.1 and 5.6.2 show. It has been reported [137, 70] that for CNTs lying on gold pads, thiol passivation affects the gold work function. This alters the Schottky barrier. Note that palladium is known to act as a catalyst for hydrogen reactions with carbon [139]. When forming a monolayer, the hydrogen of the thiol group can penetrate the palladium and diffuse to the nanotube. There hydrogen can react with the tube leading to a local destruction of the carbon network forming the tube.

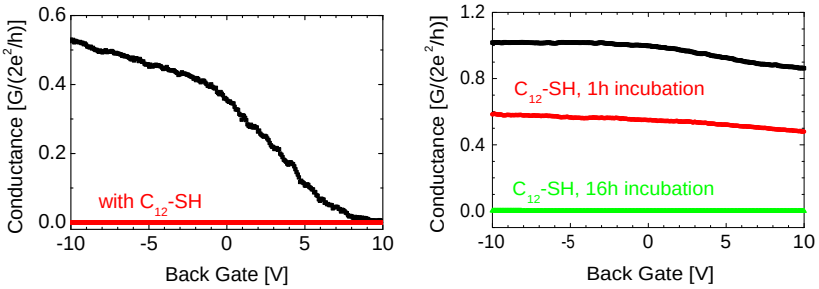


Figure 5.25: CNT FET with C_{12} thiol monolayer. (a) shows a typical example of a SWNT and (b) shows a nanotube with weak gate response before (■) incubation, after 1 h (●) and after 16 h (▲).

For the second explanation one has to consider that thiols can etch the palladium by pulling atoms away from the film [140]. Such an etching process could alter the contact at the front of the palladium. Alternatively thiols might creep between the metal contact and the nanotube. But as C_{12} thiols are big molecules and palladium is known to wet the

nanotube very well this would only affect the front side of the palladium - nanotube contact. But the contact region between the palladium and the nanotube is very long (typically $> 1\,\mu$m). If conductance at the front side of the metal - nanotube contact is suppressed one would expect the current to pass from further below the palladium. Therefore the second explanation implies that the current must pass from the metal edge to the free nanotube and cannot pass the tube section below the palladium as sketched in Figure 5.26.

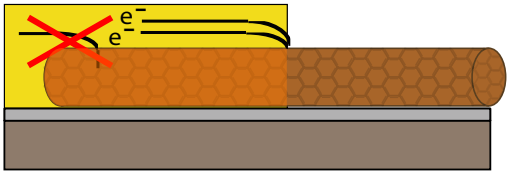


Figure 5.26: Schematics of the current flow from the metal to the nanotube. Although the contact region is long, all the current is forced in the nanotube at the metal edge. No current can flow into the tube, if the current through the front edge of the metal–nanotube contact is suppressed.

The time scale of the observed conductance suppression is very long as one can see from Figure 5.25(b). One hour of incubation reduced the conductance to slightly more than half the original value. It has to be incubated longer to totally suppress the current. It is known that hydrogen diffuses easily trough palladium and in liquid, thiol adsorption starts very quick so that one would expect a short time scale for a palladium catalysed reactions. On the other hand, the time scale to reach full coverage for a monolayer is much longer and etching is a process that occurs in thermal equilibrium and goes on even when the monolayer coverage reaches 100 %. For these reasons the timescale observed in Figure 5.25(b) speaks for explanation two (etching and edge current flow) rather than for a chemical destruction of the tube. Methoxy(poly-(ethylene glycol))thiol has been reported to have no effect on palladium contacted devices [138]. This could be explained by the fact that the kinetics of these huge molecules

are very slow and therefore etching is not efficient.

A second indication for a contact effect can be found when an alkane thiol monolayer is assembled on contacts of a multi–walled carbon nanotube and on bundles. Figure 5.27 show the effect of C_{12} and C_6 thiols on such devices. The conductance is not completely suppressed, but about two orders of magnitude below the intrinsic conductance. Interestingly it shows a semiconducting behavior where as without thiol only little effect of the back–gate can be seen. This could be explained by assuming a double walled carbon nanotube with a metallic outer and a semiconducting inner shell. Previous studies in our group showed that in a multi–walled carbon nanotube, most of the current passes within the most outer shell [141]. If the contact to the outer shell is destroyed, the inner shells can still carry a current but with much higher contact resistance. Analogous mea-

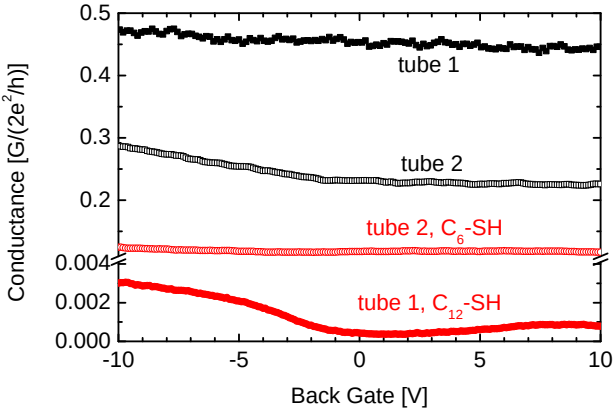


Figure 5.27: MWNT FET with thiol covered contacts. ■ and □ show tube 1 and 2 without thiols. ● shows tube 1 with C_{12}-SH and ○ shows tube 2 with C_6-SH.

surements were carried out with C_6-SH on a similar device (open squares and circles in Figure 5.27). This time the conductance is suppressed only

partially (to about 30 % of the original value). In the above mentioned picture of edge–dominated conductance, this could mean that there is still the possibility of a tunnel current through the much shorter hexane chain. Note that sufficient statistics are missing on MWTNs or bundles to firmly support the suggestions in this paragraph about MWNTs. One aspect is that we cannot be sure about having single or multi–walled tubes. (The tubes described in this paragraph come from runs with predominantely multi–walls or bundles (see Appendix C.1)). Observations are consistent with the experiments on SWNTs.

A palladium catalyzed chemical reaction of the hydrogen group of C_{12}-SH with the nanotube can be prevented by using carbon chains with a disulfide bond: $C_{12}S\text{-}SC_{12}$. This can coordinate with palladium without any hydrogen release. The $C_{12}S\text{-}SC_{12}$ was syntesized by S. Grunder of the Department of Chemistry, University of Basel. Monolayers were assembled the same way as thiol monolayers. The effect of dodecane disulfide

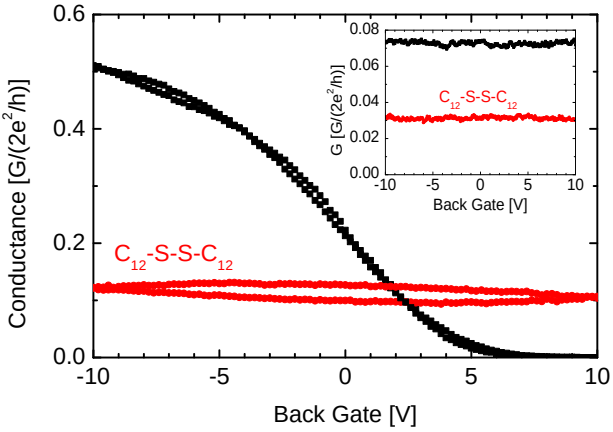


Figure 5.28: CNT FET without (■) and with (●) dodecane disulfide on contacts. Inset: same for a metallic CNT.

covered contacts on the transfer characteristic of a CNT FET can be seen in Figure 5.28. The effect seems to be the same as for dodecane thiol, but less pronounced. The inset of Figure 5.28 shows the same effect on a metallic nanotube. This means that effects cannot come of a gating effect. $C_{12}S\text{-}SC_{12}$ cannot chemically react with the nanotube. Etching in case of $C_{12}S\text{-}SC_{12}$ is expected to occur the same way as for C_{12} thiol, but slower. There are two reasons for this: The kinetics of the much larger disufides is slower than kinetics of C_{12} thiols and the disuflides are expected to bind slightly less efficiently to palladium. As the disulfides don't chemically react with the tubes we conclude that contact between the metal and the nanotube is affected by an etching process. This supports the view that current can only pass from the metal to the tube via the front edge of the contact and not via the tube below the contacts.

It has been reported previously that Pt probes on a SWNT lead to multiple quantum dots at low temperatures [142]. It follows that the two CNT segments on each side of the Pt contact are electronically separated. For Pd contacted metallic tubes with an additional Pd strip in the center of the device it has been reported first, that the conductance is limited by twice the contact resistance of the Pd and and second, that Fabry-Perot oscillations at low temperature indicate an effective CNT length corresponding to the uncovered part [143]. These two observation support the assumption that SWNTs cannot carry any current when covered with Pt or Pd. This explains why in all sensing experiments contact effects are extremely strong.

5.6.2 Surface charges on the substrate

The silicon oxide surface is polar and can be charged or dipolar molecules like water stick to it. To control these effects, the surface was made hydrophobic. For this reason a monolayer of octyl- or methyl- ended silane molecules was deposited as described in Appendix C.6. The structure of the molecules is shown in Figure 5.29. When annealing the alkanetriethoxysilane reacts with the SiO_2. The ethoxy groups are split between silicon and oxygen or between oxygen and the ethyl group and bind directly to the surface silicon or oxide group [144, 145, 146]. The unpolar

octyl- or methyl- group govern the new surface properties. Therefore water and other polar molecules are expected to be repelled from the surface. Octyltriethoxysilane and Methyltrethoxysilane show the same effect on the transfer characteristic of CNT FETs. Figure 5.30 shows the back–gate response of a CNT FET before and after passivation of the SiO_2 surface with octyltriethoxysilane. The hysteresis is not reduced but remains. The main effects are an increase in on–conductance of almost 15% and a reduction in fluctuations of hysteresis by 30%. This shows that it is important to control the surface properties of the substrate close to the nanotube because it can interfere with sensing mechanisms.

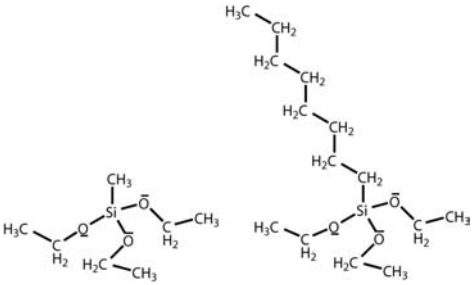
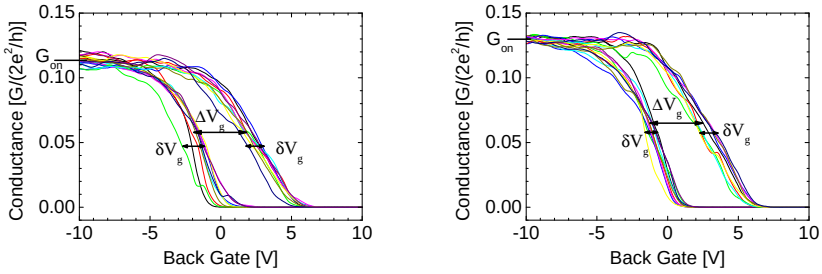


Figure 5.29: Structures of Methyltriethoxysilane (left) and Octyltriethoxysilane (right).

5.6.3 Degradation of CNT FETs

The stability of devices over long time is an important issue as sensing devices cannot be sealed completely. Therefore the conductance is measured over time. In freshly prepared devices, a decay of the on–current is often observed over time as shown in the example of Figure 5.31. After some hours it stabilizes and the sample can be used for days.

To study this decay in more details, the back–gate was repeatedly ramped from $-10\,\mathrm{V}$ to $10\,\mathrm{V}$. Figure 5.32 shows some of these ramps for a fresh device. One can clearly see that the threshold voltage is not much affected,



(a) (b)

Figure 5.30: Response to back–gate voltage of CNT FET before (a) and after surface coverage with octyltriethoxysilane (b). 10 subsequent curves, 90 s each.

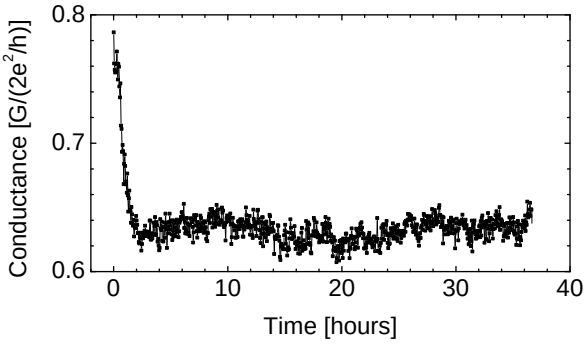


Figure 5.31: Decay of on–current in a CNT FET. Bias is 1 mV at 317 Hz. Gate is −10 V.

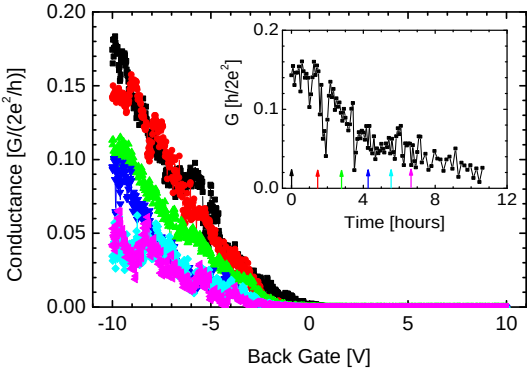


Figure 5.32: Decay of on–current in a CNT FET. The gate was repeatedly swept. Curves after 0, 1.4, 2.8, 4.3, 5.7 and 6.7 hours are shown. The inset shows for all gate ramps the value at $V_g = -9\,\mathrm{V}$.

but the on–current is reduced. It is not clear wether this decay is caused by an increasing contact resistance or by a reduction of the mobility. More details of the decay can be found in the inset of Figure 5.32. It shows the conductance value at $V_g = -9\,\mathrm{V}$ of all gate ramps of the time series. The original transfer characteristics can be reached again by functionalizing the surface with methyltriethoxysilane (for detailed recipe see Appendix C.6). This is shown in Figure 5.33. The inset shows how Methyltriethoxysilane makes the SiO_2 surface -CH_3 terminated. This shows how sensitive the CNT FET is to the surface state of the substrate oxide.

In summary we see that to enable a stable performance of CNT FET sensors in liquid, the metal - tube contacts and the substrate have to be inert. Device features are conserved when contacts are covered with PMMA or SiO_2. Alkane thiols and alkane disulfides cannot be used for passivation of palladium contacts as they destroy the metal - tube contact. We suggest that the contact metal is slightly etched by the sulfur. We suspect that the current flows from the metal edge to the tube while the tube below the palladium contact cannot conduct. Stabilization of the

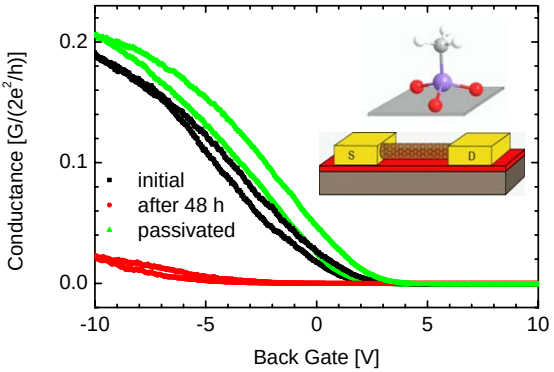


Figure 5.33: CNT FET of Figure 5.32. Black: initial behavior. Red: after 48 h decay. Green: after oxide surface is functionalized with Methyltrethoxysilane. Inset sketch of the functionalized surface.

devices can be achieved by a hydrophobic molecular monolayer on the SiO_2 substrate.

CHAPTER 6

Final comparison and outlook

In this chapter we summarize the work by comparing SiNW and CNT FETs. Focus is set in their suitability for sensing purpose. Fabrication issues, transistor behavior, stability issues and environmental effects are considered in the following sections. As a conclusion some suggestions for future device design and an outlook are given in Section 6.4.

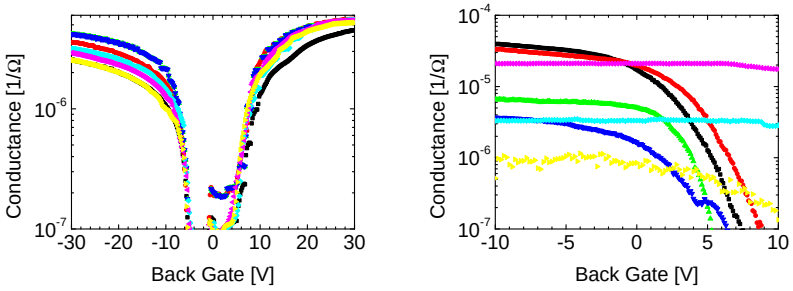
6.1 Fabrication Issues

The "top–down" approach for fabrication of SiNW FETs described in Chapter 3 is a parallel process that could easily be scaled to wafer production. The only serial step is the e-beam lithography of the wires itself. As these are individual short lines, the writing time is extremely small.

The fabrication process is fully CMOS compatible which would allow integration of on–chip electronics. The only critical issue is the control over nanowire width. In our case most variation come from lithography and TMAH etching. The width of the mask depends very much on the focus of the e-beam which is adjusted manually. This problem can be overcome by choosing a writing width that does not approach the machines limits. This can be done if the nanowire width can be controlled by under etching the mask. This requires good control over the TMAH etching process including orientation along crystalline planes.

The fabrication scheme describe in Chapter 3 for producing CNT FETs is relatively robust as tubes are selected individually. Thanks to the good quality of CNTs grown by the developed CVD process, good device characteristics can be reached such as high on–current and clear off state. The fabrication scheme allows avoiding post growth processing of CNTs which helps us to make use of this high quality. An intrinsic problem of CNT FETs is the fact that in CVD growth a wide distribution of tube chiralities with different electronic properties are present. The disadvantages of the described fabrication scheme is that the high temperatures involved in the CVD growth on substrate are not CMOS compatible and that selecting and contacting tubes individually is very time consuming.

Device to device variations for both device types are shown in Figure 6.1. In case of CNT FETs about one forth of devices was not working. Seven devices were chosen from a single fabrication series in both cases, avoiding non–working devices for CNT FETs. All the SiNW FETs overlap quite well with some variation in conductance for high gate voltage reaching $\pm 30\,\mathrm{V}$. Out of the presented CNT FETs four show semiconducting and two show metallic behavior where as one device with very low maximal conductance shows weak gate dependance. Such variations are typical for wide distribution of grown CNT types. This is not fundamentally limiting when studying CNT FETs for scientific purpose but causes increasingly problems when moving towards application.



(a) (b)

Figure 6.1: Variation between different FETs produces in one batch for seven SiNWs (a) and seven CNTs (b).

6.2 Transistor behavior

SiNW FETs that are not thinner than the screening length L_D can be described by the standard MOSFET model considering a modified gate capacitance C_g and limited depletion capacitance $C_d^{NW} > 2 \cdot 10^{-3}\,\mathrm{F/m^2}$. The latter leads to an improved subthreshold swing. For CNT FET a simple model considering the quantum capacitance is given in Section 2.3. The transistor behavior of SiNW FETs and CNT FETs is described in Chapter 4 by detailed study of some example devices. In Table 6.1 some device parameters are compared by typical values for a dozen of both kind of devices.

High variation in effective device mobilities come from the fact that they depend on series resistances of lead in case of SiNW FETs and contacts in case of CNT FETs. The highest observed electron device mobility $\mu_{dev,e}$ is as high as the electron mobility in low doped bulk silicon. Note that the analysis of subthreshold swings tends to too high values and has high error because of the small dynamic range in typical measurements. Low subthreshold swings as observed here show the good quality of our devices

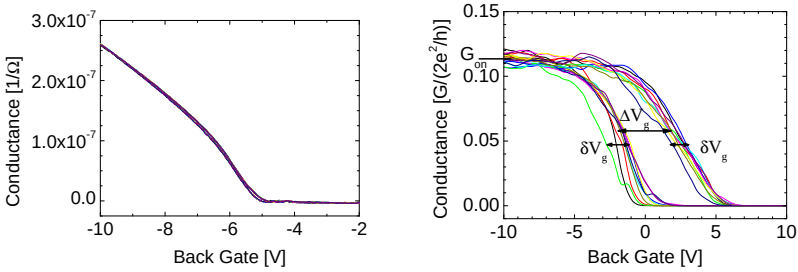
Table 6.1: Typical device parameters of SiNW and CNT FETs

	SiNW FETs	CNT FETs
$V_{th}, p-side$	$-7\ldots-4.5\,\mathrm{V}$	$-5\ldots9\,\mathrm{V}$
$\mu_{dev,h}$	$50\ldots200\,\mathrm{cm}^2/(\mathrm{Vs})$	$100\ldots2500\,\mathrm{cm}^2/(\mathrm{Vs})$
$\mu_{dev,e}$	$200\ldots1400\,\mathrm{cm}^2/(\mathrm{Vs})$	
$S = dV_g/d(\log(G))$	$70\ldots700$ mV/dec	$< 200\,\mathrm{mV/dec}$ for 50 %
		$0.5\ldots2\,\mathrm{V/dec}$ for 50 %

which means low trap state density and low Schottky barriers.

For back–gate voltages below $\sim 6\,\mathrm{V}$ beyond V_{th} the conductance of CNT FETs saturates. This saturation is dominated by the quantum conductance for four channels and contact resistances and typically lies in the range of $G_{sat} \sim 0.1-1\cdot 2e^2/h$ (corresponds to $\sim 10-200\,\mathrm{k\Omega}$) which is very high for typical semiconducting CNTs. In case of SiNW FETs no saturation in conductance is observed for back–gate voltages up to $\pm 30\,\mathrm{V}$ that were in use. Typical resistances are in the range of $1\,\mathrm{M\Omega}$ for $V_g = -10\,\mathrm{V}$. In SWNTs current saturation for high bias voltages is around $25\,\mu\mathrm{A}$. For SiNW FETs current saturation is more device dependent. Up to $1\,\mu\mathrm{A}$ the current is very linear with bias, but it can deviate above.

Hysteresis in back–gate response is small in SiNW FETs and originates from surface effects (Section 4.1.7). CNT FETs typically show very pronounced hysteresis. It comes at least partially from the contact region and can be reduced by an annealing step before contacting (Section 4.2.4). Fluctuation in back–gate response are very high for any time scale in case of CNT FETs, but much lower for SiNW FETs. To show this the accumulation region of a series of 10 curves is plotted in Figure 6.2 for both type of devices. The small hysteresis and high stability of the SiNW FET is in obvious contrast to the case of CNT FET.



(a) (b)

Figure 6.2: Fluctuations in back–gate response of SiNW (a) and CNT (b) FETs. Accumulation region of 10 subsequent curves in both cases ramping V_g from -10 to 10 V and back, 90 s each ramp.

6.3 Sensing with Nano FETs

Sensitivity of CNT FETs is very high for charge transfer from molecules to the CNT (Section 5.5.1), for an electric field of nearby ions (Section 5.5.2) or even non charged dipolar molecules (Section 5.5.3). Electrolyte gating efficiency is about 200 times higher than back–gate efficiency. For SiNW FETs the gating efficiency is about 6 times higher for electrolyte–gate. In the design of SiNW FETs semiconducting leads are introduced between the nanowire and the metal contact. This allows a separation of bulk nanowire effects and contact effects. By the combination of back–gate and electrolyte–gate, the devices can be tuned in regions where the nanowire is current limiting and in regions where the contact regions are current limiting.

The conductance of SiNW FETs shows very robust sensitivity to pH variations when modulating back–gate and electrolyte–gate. We point out that only controlling both, back–gate and liquid potential can lead to well defined sensing experiments, as the effect of pH variation and variation in liquid potential superpose. Nanoscale FETs require very small

volumes and are sensitive to a small amount of analyte molecules. Note that when speaking about sensitivity, we refer to response in conduction to the electronic potential built up by the analyte on the surface. This scales with the mobility μ and the semiconductor capacitance C_s. The sensitivity of SiNWs could be enhanced by removing the top oxide locally on the SiNW and narrowing down its diameter [147, 106]. This could be reached by controlled etching as described in Section 6.1. The use of Si (110) wafers would allow vertical side walls in TMAH etching (see Appendix C.1). This way the widened bottom part of the SiNWs could be avoided. CNT FETs are intrinsically very sensitive because of their high mobility and because transport is dominated by a small number of carriers. Note that fluctuation in number of carriers dominate noise in CNT FET sensors [148]. This means they reach the fundamental limit in FET sensing. In SiNW FET sensors an optimum of sensitivity vs. noise can be found adjusting the NW size depending on the application of interest.

Fluctuation in transfer characteristic of CNT FETs can be reduced by passivation of the SiO_2 substrate with a hydrophobic molecular layer. But CNT FETs are very unstable when exposed to liquids. Palladium - tube contacts can be attacked easily which completely destroys conduction of nanotubes. SiNWs on the other hand are very stable, not only in air but in liuqid as well (see Section 5.3.3). More effort has to be put into stable measurement setup. As no optimization on stability has been performed we don't directly compare them to highly optimized ISFET devices. But we expect that stability of SiNW FETs could be improved beyond the known standard of ISFETs for two reasons: First, the high sensitivity should allow more flexibility in chemically functionalizing and protecting the devices. Second, high electrolyte–gate voltages could be avoided because the back–gate can be used to tune the device into a sensitive region. The lower the applied voltages are, the less they can drive a degradation of the devices.

6.4 Summary and Outlook

SiNW FETs and CNT FETs have been studied as candidates for integrable biosensors. Both types show sensing capability, CNT FETs even for uncharged molecules. The "top–down" process developed for SiNW FET fabrication gives much freedom in device designing and is fully compatible with CMOS production schemes. Due to the fact that the SiNW fabrication reported here uses the same structuring techniques as in CMOS processing, it is very reliable. The fabrication of CNT FETs is based on CVD. By this process CNT FETs with interesting device parameters can be reached. Since CVD needs high temperatures it is not compatible with CMOS techniques. CVD growth leads to a mixture of CNT types which results in a low device yield. The contact regions between the nanoscale CNTs and fabricated metal contacts are very critical. Hysteresis, device break down due to metal etching or chemical disruption and instability in liquid environment have been attributed to the Pd–CNT contacts. It was shown that the degradation of CNT FETs can be recovered. With this both device types show good long term stability. The concept of combining the electrolyte–gate with the back–gate, presented in the example of pH sensing on SiNW FETs, enables stable performance in liquid environment.

Based on our current experience we propose the following improvements regarding future device design:

SiNW FETs

- Improvement in sensitivity could be reached by removing the top oxide locally and by reducing the nanowire width. An optimal width needs to be found for high sensitivity and low device to device fluctuations.

- A higher doping, up to $\sim 10^{18}\,\mathrm{cm}^{-3}$, would enhance the contact properties and lower the threshold voltages. But as the screening length L_D is reduced, the nanowire width has to be reduced as well.

- Control of the nanowire surface by a thin oxide layer or covalent functionalization could help for stabilization and would allow specific sensing.
- Differential measurements between a sensing and a reference SiNW FET would allow stable performance.

CNT FETs

Especially with respect to stability and to reproducibility further improvements need to be done. Some possible solutions are:

- Humidity free fabrication and annealing before the deposition of the metal contact.
- Titanium as contact material. Annealing leads to titanium carbide contacts [32] which are less transparent, but expected to be more stable.
- Contact passivation has to be very robust and innert. Therefore we suggest to cover the contact region with silicon oxide or silicon nitride.
- Increase of the hydrophobicity of the SiO_2 surface by a monolayer of alkane ended molecules.

Due to the improved stability in fabrication and performance reported here and with the further improvements suggested above, we can think about possible applications of SiNW FETs and CNT FETs and give an outlook on possible future developments.

The high intrinsic sensitivity of CNT FETs is of interest in real time monitoring of minute amount of molecules — or ultimately single molecules — without labelling. In contrast to conventional sensing techniques, such as fluorescence microscopy, the devices can easily be integrated on a micro chip which is of special interest for *in vivo* experiments where access

with optical instruments is limited. Need in current basic research of biophysics can be met this way. However the limited reliability in fabrication and performance of CNT FETs hinders their integration into complex, highly integrated devices or their implementation in industrial products. In contrast to this SiNWs are well suited in this respect. The fabrication is entirely CMOS compatible and very flexible in design. Devices proved to be robust under the conditions of all performed experiments. Depending on the application of interest the sensitivity can be chosen by adjusting the NW size. The SiNW FETs introduced here can be used as transducers for various sensor types. Implementing on–chip micro pH sensors would be the most direct way to an industrial product. For this purpose, two different surface types are needed: a pH–sensitive surface for the working FET and a pH–insensitive surface for a reference FET. Going beyond this into the field of biosensing, specific receptors have to be immobilized. For multiplex sensing, each SiNW in an array has to be functionalized individually. This can be realized by techniques such as microcontact printing [149], dip-pen- [150] or conventional lithography [151] combined with UV assisted Si-H chemistry [152] or by electrical addressing of individual NWs, for example by electrochemical [153] or local heat assisted [154] Si chemistry. In a next step the SiNW sensor array has to be combined with an electronic read out system — preferably implemented on–chip. Further on such a multiplex sensor device can be integrated in a micro fluidic system. Complex micro fluidic systems including actuators such as pumps and valves, separation and mixing chambers, and liquid multiplexing, all on one chip have been reported [155, 156, 157, 158]. Integrated sensors that can be coupled to actuators via integrated electronic control elements can enhance the functionality of such devices. As an example we think of a ring mixer where the liquid is cycled repeatedly. An integrated sensors could not only monitor the mixing, but the product of chemical reactions in situ. Combining the sensors, logic on–chip electronics and micro fluidic actuators would lead to complex, even programmable Lab-On-Chip systems. Such devices could be used for fast and massively parallel analyzing tools — maybe a key technology for systems biology and an opening to the “post microarray area”.

APPENDIX A

Electronic properties of CNTs

In this section we describe the electronic properties of single–walled carbon nanotubes (SWNTs) with the aim to derive the energy dispersion and the density of states which we need in the model of carbon nanotube FETs described in Section 2.3. We start with the structural properties, then derive the band structure of graphene and carbon nanotubes (CNTs) and conclude with the density of states. A very good introduction into the properties of carbon nanotubes can be found in [159].

A.1 Structural properties of CNTs

The microscopic structure of carbon nanotubes is closely related to a single two-dimensional layer of graphite, so-called graphene. Therefore graphene

is the starting point for a description of carbon nanotubes. One can look at them as a sheet of graphene rolled up into a hollow cylinder with a diameter in the range of one or two nanometers. There are infinitely many ways to roll a sheet into a cylinder, resulting in different diameters and microscopic structures of the tubes. These are defined by the chiral vector $\vec{c}$.

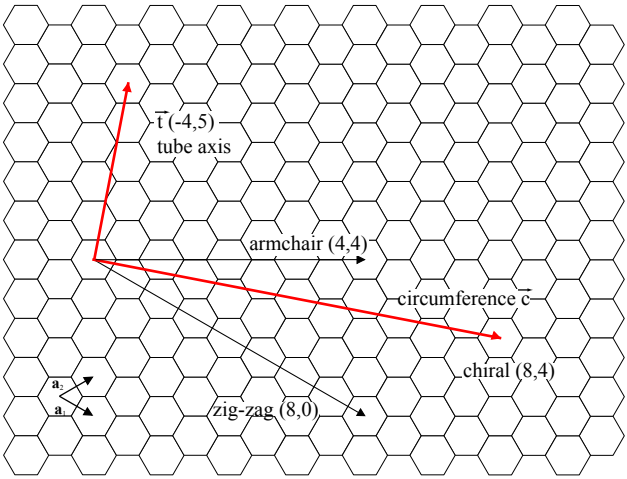


Figure A.1: Graphene honeycomb lattice with the lattice vectors $\vec{a}_1$ and $\vec{a}_2$. The chiral vector of an armchair and a zig-zag tube are indicated. The chiral vector $\vec{c}$ of a (8,4) tube and the corresponding tube axis $\vec{t}$ are indicated in red.

Figure A.1 shows the graphene honeycomb lattice. The unit cell is spanned by two vectors $\vec{a}_1$ and $\vec{a}_2$ that form an angle of 60° and length $|\vec{a}_1| = |\vec{a}_2| = a_0 = \sqrt{3}a_{CC}$ where $a_{CC} = 1.42$ Å is the nearest neighbor C-C bonding distance. The graphene unit cell contains two carbon atoms at the positions $\frac{1}{3}(\vec{a}_1 + \vec{a}_2)$ and $\frac{2}{3}(\vec{a}_1 + \vec{a}_2)$. In carbon nanotubes, the graphene sheet is rolled up in such a way that a graphene lattice vector $\vec{c} = n_1\vec{a}_1 + n_2\vec{a}_2$ be-

comes the circumference of the tube. This circumferential vector $\vec{c}$, which is usually denoted by the pair of integers (n_1, n_2), is called the chiral vector and uniquely defines a particular tube. In Figure A.1 the example (8,4) for the chiral vector $\vec{c}$ is indicated by a red line. As predicted by Mintmire, Dunlap and White [160] the electronic properties of nanotubes depend drastically on the chirality, even for tubes with similar diameter. There are two special cases: Tubes of type $(n, 0)$ are called zig-zag tubes, because they exhibit a zig-zag pattern along the circumference, and (n, n) tubes are called armchair tubes. Examples are shown in Figure A.2.

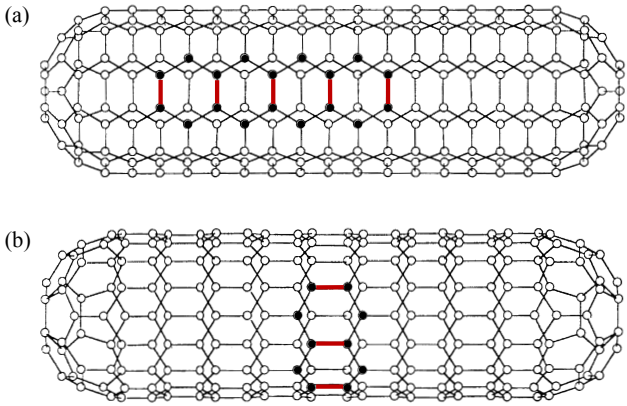


Figure A.2: Structure of the lattice of a zig-zag (a) and an armchair (b) tube. For clarity some C-C bonds perpendicular (a) and parallel (b) to the tube axes are marked (Adapted from [161]).

The geometry of the graphene lattice and the chiral vector of the tube determine its structural parameters like diameter, unit cell and its number of atoms, as well as the size and shape of the Brillouin zone. The diameter of the tube is given by the length of the chiral vector:

$$d = \frac{|\vec{c}|}{\pi} = \frac{a_0}{\pi}\sqrt{n_1^2 + n_1 n_2 + n_2^2}. \tag{A.1}$$

The smallest graphene lattice vector $\vec{t}$ perpendicular to $\vec{c}$ defines the translational period t along the tube axis. This corresponds to the vector (-4, 5) in the example of Figure A.1. The unit cell of the nanotube is defined as a cylindrical surface with length t and diameter d.

A.2 Electronic properties of Carbon Nanotubes

A.2.1 Overview

In carbon nanotubes as well as in graphene each carbon atom has three σ-bonds to its neighboring atoms. These electrons are strongly bound and do not play a role in electronic transport or optical absorption in the visible energy range. The fourth carbon valence electron contributes to electronic π-bands extended over the whole system. In a carbon nanotube the electron wavelength around the circumference is quantized due to periodic boundary conditions – only a discrete number of wavelengths can fit around the tube. Along the tube the electrons are not confined. Because of the quantization of circumferential modes, the tube's electronic states do not form one wide electronic energy band, but instead split into one-dimensional subbands with band onsets at different energies. For single-walled nanotubes, these subbands are widely separated in energy, on the scale of 1 eV. There are two cases: the allowed wavevectors $\vec{k}$ do not or do pass through the Fermi points of graphene where the conduction and valence bands meet. If the first case occurs, we have a semi-conducting carbon nanotube with a band-gap of the order of 1 eV. If the second case occurs, we have a metallic nanotube where only two of the one-dimensional subbands cross the Fermi energy causing a limited conductance of $4e^2/h$, the so-called quantum conductance. The condition for being metallic is given by $n_1 - n_2 = 3\nu$ for any integer ν. This approach of calculating subbands of the graphene band structure, is called zone folding approach. For more detailed band calculations, curvature effects have to be included, especially for small diameter tubes and electronic states far from the Fermi

level. This will not be considered here, but in the following sections we will explain the zone folding approach in more details.

A.2.2 Graphene

The unit cell of graphene builds up a hexagonal lattice and its reciprocal lattice is hexagonal again. Figure A.3(a) shows the Brillouin zone of graphene. The dispersion relation $E(k)$ can be calculated from a tight-binding model [162]:

$$E(\vec{k})_{graphene} = \pm\gamma\sqrt{1 + 4\cos\left(k_x\frac{3a_{CC}}{2}\right)\cos\left(k_y\frac{\sqrt{3}a_{CC}}{2}\right) + 4\cos^2\left(k_y\frac{\sqrt{3}a_{CC}}{2}\right)} \tag{A.2}$$

where $\gamma \approx 3.0\,\text{eV}$ is the C-C bonding energy. The positive sign gives the conduction band and the negative sign the valence band as shown in Figure A.3(b). The two bands intersect at $E = 0$ at the six corners of the Brillouin zone. Because of this special property of graphene it is somtimes called a zero-gap semiconductor. The six corners of the Brillouin zone are given by

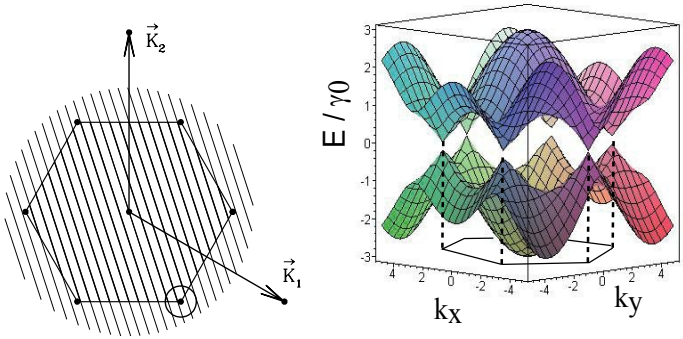
$$\vec{k}_{corner} \equiv \pm(\vec{b}_1 - \vec{b}_2)/3, \quad \pm(2\vec{b}_1 + \vec{b}_2)/3 \quad \text{and} \quad \pm(\vec{b}_1 + 2\vec{b}_2)/3 \tag{A.3}$$

where $\vec{b}_1$ and $\vec{b}_2$ are the basis of the reciprocal lattice given by $\vec{b}_i \cdot a_j = 2\pi\delta_{ij}$.

A.2.3 Band structure of Carbon Nanotubes

The simplest way to obtain the band structure of a carbon nanotube is to begin with the bandstructure of graphene and apply periodic boundary conditions along the circumference.

$$\vec{k} \cdot \vec{c} = 2\pi\nu, \tag{A.4}$$



(a) (b)

Figure A.3: (a) Hexagonal central Brillouin zone of graphene. Parallel lines depict allowed states for a (13, 6) SWNT. The circle at bottom right encloses the region of states near E_f (adapted from [163]). (b) Band structure of graphene. The valence and conduction bands meet at six points corresponding to the corners of the first Brillouin zone (adapted from [164]).

with an integer ν. This boundary condition is understood in the following way: The wave function of an electron (or a phonon) must have a phase shift of an integer multiple of 2π around the circumference. All other wavelengths will vanish by interference. In terms of the two-dimensional Brillouin zone of graphene, the allowed states will lie along parallel lines separated by spacing of $2\pi/|\vec{c}|$ as indicated in Figure A.3(a). If one of these lines passes through the Fermi point, we have a metallic nanotube, if not we have a semiconducting one. To calculate the condition for passing the Fermi point we plug the expression A.3 for the Fermi points and the chiral vector $\vec{c} = n_1\vec{a}_1 + n_2\vec{a}_2$ into the boundary condition (A.4): $\vec{k}_{corner}\cdot(n_1\vec{a}_1+n_2\vec{a}_2) = 2\pi\nu$. Remembering the definition of the reciprocal lattice vector $\vec{b}_i \cdot a_j = 2\pi\delta_{ij}$ we get

$$2\pi\nu = \vec{k}_{corner} \cdot (n_1\vec{a}_1 + n_2\vec{a}_2) = 2\pi(n_1 - n_2)/3 \tag{A.5}$$

for all the six corner points. And therefore the simple condition for nanotubes to be matallic

$$n_1 - n_2 = 3\nu \tag{A.6}$$

for any integer ν. With curvature effects included it can be shown that only the armchair SWNTs are truly metallic [160]; all other SWNTs satisfying the metallic condition are quasimetallic with small band gaps varying as the inverse square of the SWNT radius.

A.2.4 Band structure near the Fermi points

For carbon nanotubes we prefer a coordinate system for the reciprocal vectors that is based on the axial vector $\vec{t}$ and the circumferential vector $\vec{c}$. We are interested in the band structure near the Fermi point. For this reason we put the origin of the new coordinate system to the Fermi point, so that the new wave vector becomes

$$\vec{k}' = \vec{k} - \vec{k}_F = k'_\perp\vec{c} + k'_t\vec{t}. \tag{A.7}$$

k'_t is the wavevector along the axis of the nanotubes. The component $k'_\perp$ along the circumferential direction, which is quantized by the periodic

boundary condition, is given by the projection of $\vec{k}'$ to the unity vector in chiral direction:

$$k'_{\perp,\nu} = (\vec{k} - \vec{k}_f) \cdot \frac{\vec{c}}{|\vec{c}|} = \frac{\vec{k} \cdot \vec{c} - \vec{k}_f \cdot \vec{c}}{|\vec{c}|} = \frac{2}{d}\left[\nu - \frac{n_1 - n_2}{3}\right]. \tag{A.8}$$

The last expression is gained from $|\vec{c}| = \pi d$ and Equations A.3 and A.4.

Since we are interested in the band structure $E(\vec{k})$ near the Fermi point we can simplify Equation A.3 for the $E(\vec{k})$ relation of graphene by using Taylor series expansion for the cosine function near the Fermi point [163].

$$E(\vec{k}) = \frac{3a_{CC}\gamma}{2}\sqrt{(\vec{k}_x - \vec{k}_{Fx})^2 + (\vec{k}_y - \vec{k}_{Fy})^2} = \frac{3a_{CC}t}{2}\left|\vec{k} - \vec{k}_F\right| \tag{A.9}$$

We see that $E(\vec{k} - \vec{k}_F)$ is linear near a Fermi point. This linear approximation holds within an energy range of $\sim 1\,\mathrm{eV}$. We are going to use this simple expression for $E(\vec{k})$ to derive the bandgap and density of states. We rewrite the linear band approximation (Equation A.9) using the coordinate system for the tube (Equation A.7):

$$E(\vec{k}) = \frac{3a_{CC}\gamma}{2}\sqrt{{k'_{\perp,\nu}}^2 + {k'_t}^2}. \tag{A.10}$$

The lowest band of the CNT is determined by the minimum value of $k_{\perp,\nu}$. We consider the cases for metallic and semiconducting tubes seperately.

Metallic Carbon Nanotubes

Carbon nanotubes are metallic if $(n_1 - n_2)/3 = \nu$, $\nu \in \mathbb{R}$ (see Equatoin A.6). In this case the component of $\vec{k}$ in circumference direction can be zero, as can be seen in Equaton A.8. The $E(\vec{k})$ relation from Equation A.10 then becomes

$$E = \pm\frac{3a_{CC}\gamma}{2}\vec{k}'_t. \tag{A.11}$$

This is a one-dimensional linear dispersion relation for the lowest band, independent of (n_1, n_2) as shown in Figure A.4(a).

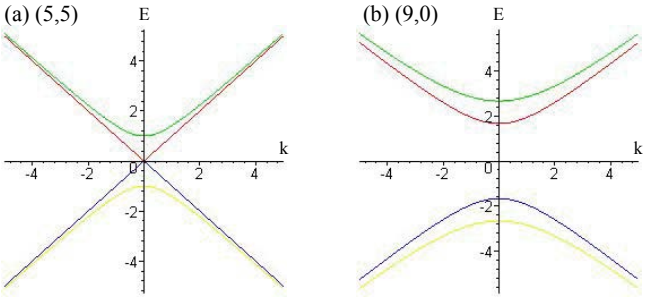


Figure A.4: Energy dispersion of (a) a metallic (5,5) and (b) a semiconducting (9,0) carbon nanotube. Energy is plotted in units of $E_0 = 2\hbar v_F/d$ and k in units of $k_0 = 2/d$ (adapted from [164].

Semiconducting Carbon Nanotubes

For semiconducting carbon nanotubes $(n_1 - n_2)/3 \neq 0$. In this case the minimum value of the circumferential wave vector is found from Equation A.8 $k_{\perp,\nu} = \frac{2}{3d}$. By substituting this expression into the linear $E(\vec{k})$ approximation for CNT (A.10) we get

$$E(k_t') = \pm\frac{3a_{CC}\gamma}{2}\sqrt{k_t' + (2/3d)^2}, \tag{A.12}$$

which is a one-dimensional dispersion relation $E(k)$ as shown in Figure A.4(b). It does not depend on the chiral numbers n_1 and n_2, but only on the diameter d. It is parabolic with a direct band gap

$$E_g = \frac{2a_{CC}\gamma}{d} \approx \frac{0.8}{d\,(\text{in nm})}\,\text{eV}. \tag{A.13}$$

A.2.5 Density of States in Carbon Nanotubes

An important quantity in transport properties is the density of electronic states (DOS). The DOS for one-dimensional systems is dominated by di-

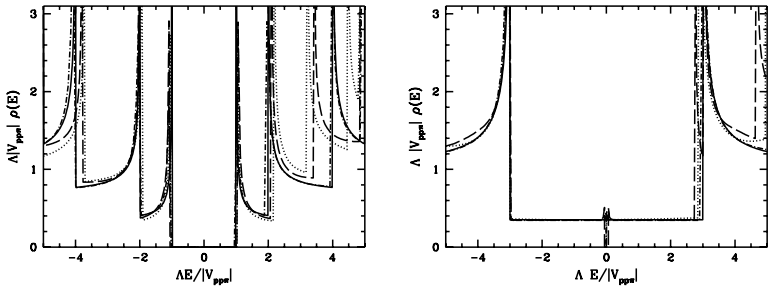
vergences, the so called van Hove Singularities. For parabolic bands it goes with $1/\sqrt{E}$ [3]. The density of states for a metallic and a semiconducting carbon nanotube is plotted in Figure A.5. In the case of a metallic nanotube it has a constant value near the Fermi energy. In case of a semiconducting carbon nanotube the density is zero in an energy gap given by Equation A.13. For both cases, we see contributions to the DOS from higher subbands that arise from different values of ν. The DOS for the lowest band of a semiconducting carbon nanotube is given by [163]

$$\mathrm{DOS}(E) = \frac{8}{3\pi a_{CC}\gamma} \frac{|E|}{\sqrt{E^2 - (E_g/2)^2}} \Theta(|E| - E_g/2), \tag{A.14}$$

where $\Theta(x)$ is the step function which equals 1 for $x > 0$ and 0 otherwise. Note that this is a density per energy and per length of the nanotube. A saturation value can be given for energies well above the band edge where $|E|/\sqrt{E^2 - (E_g/2)^2}$ goes towards one:

$$\mathrm{DOS} = \frac{8}{3\pi a_{CC}\gamma} = 2.0 \cdot 10^9 \, \frac{1}{\mathrm{eV\,e}} \qquad \text{for} \quad E \gg E_g/2 \tag{A.15}$$

which corresponds to the density of states of the linear dispersion relation (see Equation A.11) of a metallic nanotube.



(a) (b)

Figure A.5: Electronic density of states for a metallic (a) and semiconducting (b) CNT. The full line is calculated by summing over all the subbands assuming an universal DOS as described in Equations A.14 and A.15. Compare to ab-initio calculations for (a): (16,9) dotted line, (16,6) dashed line, (21,20) dot-dashed line and (b): (10,10) dotted line, (14,5) dashed line and (22,19) dot-dashed line. The energy and the DOS were scaled with the parameter $\Lambda = d/a_{CC}$. From [163].

APPENDIX B

Supporting measurements

In this Appendix details about perviously explained measurements and some supporting measurements are presented. The context for each presented graph can be found in the Sections referred to in the figure captions.

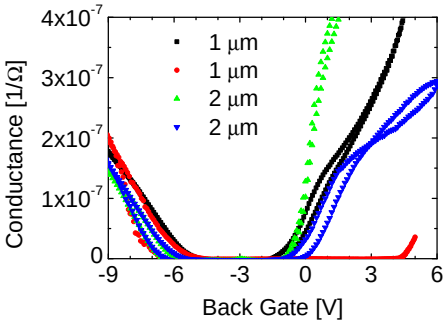


Figure B.1: Dependance of transconductance on NW length for short SiNW FETs. Width is $\sim$ 100 nm for all. One can see that in accumulation there is very little variation. In inversion variations show no dependance on length. The conductance of these devices seems do be dominated by leads and contacts. This is different for long NWs as shown in Figure 4.11.

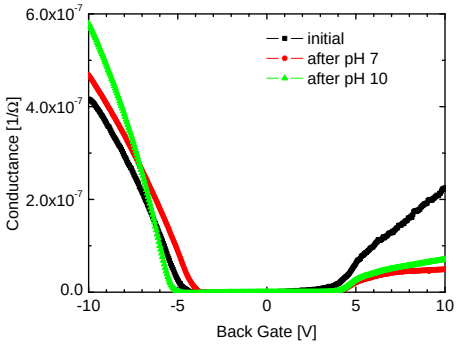


Figure B.2: G vs. V_g in air for sample of Figure 5.16. Before first measurement, after pH 7 measurement and after pH 10 measurement. There is no systematic drift. This supports that the measured effect of Figure 5.16 and Figure 5.17 are real sensing effects.

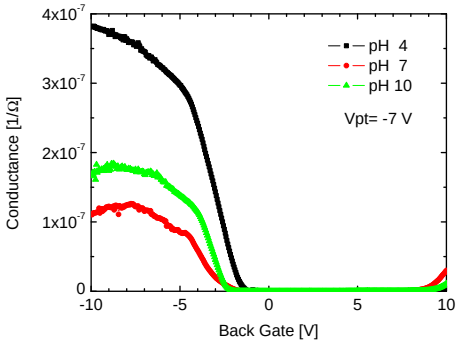


Figure B.3: G vs. V_g in 1 mM KCl at pH 4, 7 and 10. Platinum electrode potential $V_{pt} = -0.7\,\mathrm{V}$. This is deduces from the measurement shown in Figure 5.16.

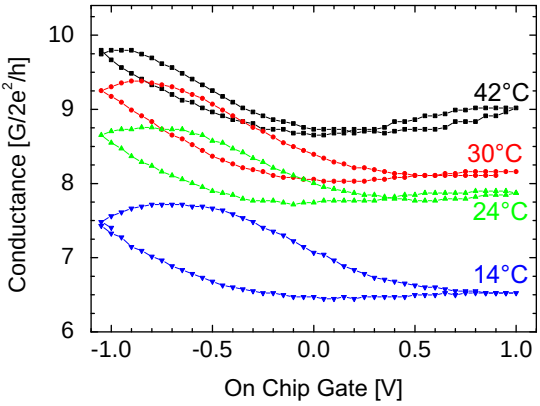


Figure B.4: Transfer characteristics of a CNT bundle FET gated by an on-chip gate. The device was exposed to the liquid crystal 5CB. Reorientation of this dipolar molecules leads to the gating effect. The hysteresis as function of temperature is shown in Figure 5.16.

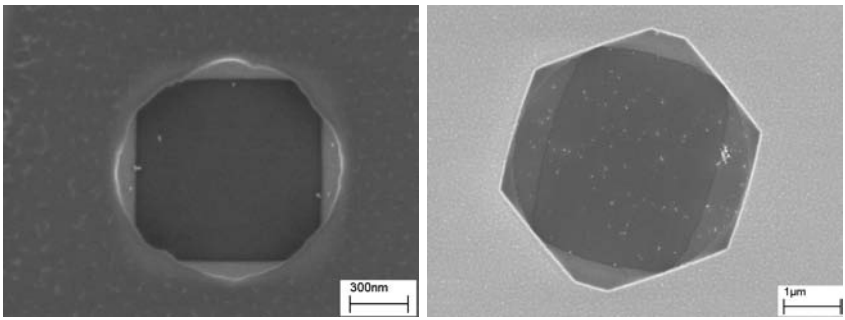
APPENDIX C

Methods

C.1 TMAH etching

To show the anisotropy of TMAH etching circles were written on Si (100) and Si (110) wafers by e-beam lithography. The top oxide of 100 nm was removed by CHF_3 plasma. Then the underlying Si was etched by TMAH (25% in water, plus 10% 2-propanol at 45° C) for 3 min. The SEM image in Figure C.1(a) shows the etching in a Si (100) wafer. The ⟨110⟩ directions are oriented vertically and horizontally in the image. {111} planes are etched much slower than the {100} planes [36]. Therefore the circular structure of the SiO_2 mask is under etched into a structure limited by {111} planes. These are perpendicular to each other, oriented in ⟨110⟩ directions, but not perpendicular to the (100) surface plane [33]. This can nicely be seen in Figure C.1(a). When etching a Si (110) wafer there are

slow etching {111} planes perpendicular to the surface but they are not perpendicular to each other. In addition there are four {111} planes that are not perpendicular to the surface ending in a six corner structure [33] as one can see in Figure C.1(b) [165]. To generate very thin nanowires perpendicular side walls would be favored as Figure C.3 shows. This requires working with Si (110) SOI wafers.



(a) (b)

Figure C.1: Anisotropy of TMAH etching with circular pattern on Si (100) in (a) and Si (110) in (b).

Etch rates depend very critically on temperature as shown in Figure C.2. This dependance is much more pronounced for small etching times. This is where the offset in the linear fit comes from. For 45° C this offset is small which means that the etch rate is constant for all the tested etching times of 20 s - 10 min. When etching at low temperature etched surfaces are very rough. Adding 2-propanol helps to wet the surface [166, 167] which leads to smoother surfaces as shown in Figure C.4. Constant stirring helps to ensure quick diffusion from the surface which is important to reach homogeneous etching.

The etch rate for TMAH (25% in water) with 10% 2-propanol at 45° C is 95 nm/min for Si (110) and 72 nm/min for Si (100). Note that the etching rate can be increased by decreasing the concentration and depends critically on boron or phosphor doping [36].

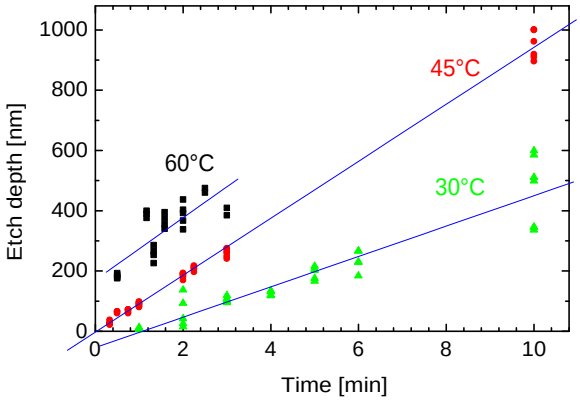
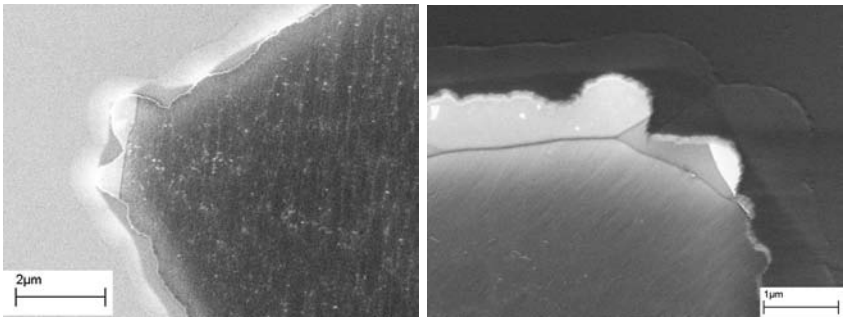


Figure C.2: TMAH etch rate for Si (110). Etch rate and offset from linear fit for 60° C (■): 103 nm/min and 170 nm offset. For 45° C (●): 95 nm/min, -3 nm offset. For 30° C (▲): 50 nm/min, -55 nm.

Figure C.3: SiNWs etched in a Si (110) wafer. Etch stops on vertical {111} planes.



(a) (b)

Figure C.4: Surface roughness of etch tests on Si (110). (a) at 60° C and (b) at 45° C with 10% 2-propanol added. This helps to smoothen etched surfaces.

C.2 Chemical Vapor Deposition of Carbon Nanotubes

The basics of CVD growth and the system used is described in Chapter 3. The parameters that can influence the growth of the nanotubes are: the time of growth, the temperature, the pressure and flow rate of the methane. The tools we have to analyse the nanotubes are limited to SEM and AFM for geometrical characterisation and electrical characterisation. The latter is very time consuming and cannot be used to optimize the set of growth parameters. Therefore we used parameters related to the ones from literature [62] and changed the temperature only as our earlier studies showed that this is the most critical parameter to tune the character of the nanotubes.

The gas system is operated at 0.1 bar relative. The flow rates for the protective gas (Ar, $>$ 99.9999% (Carbagas Quality No. 60)) and the reaction gas CH_4 ($>$ 99, 9995% (Carbagas Quality No. 55)) are 60 l/h. The flow meters are gauged to air, with the correction factors 0.85 (Ar) and 1.34 (CH_4) the flow rates are effectively 850 sccm/min for Ar and

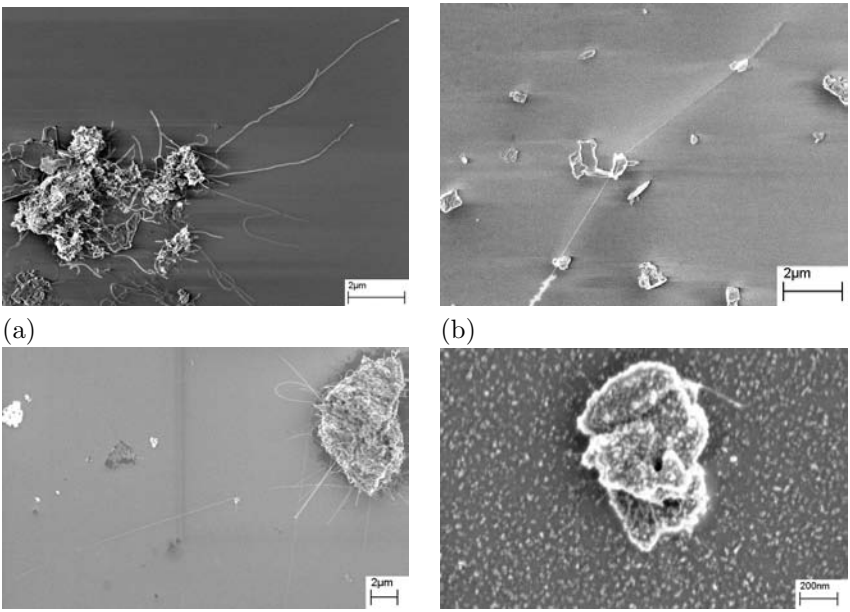
1340 sccm/min for CH_4, respectively. The time of growth is fixed to 10 min. Hydrogen ($> 99,9999\%$, 500 sscm/min) is added during and after growth. It reduces the deposition of amorphous carbon, but it competes with the growth process [63]. Therefore the flow of hydrogen was chosen moderately. To prolong the time of growth is not expected influence the tubes as growth times are in the region of seconds. But much shorter growth times of 2 min resulted in less tubes.

We swept temperatures from 850° C to 1100° C which seems to be the interesting region, see Figure C.5. For lower temperatures double- or multi–walled nanotubes are dominant. For temperatures around 900° C and below we saw only short tubes near catalyst particles. We could not find any straight ones. For temperatures between 950° C and 1000° C the tubes look much longer and straighter. For temperatures above 1000° C amorphous carbon sticks on the surface. We guess that bent and kinked tubes have more defects and straight ones have less. Hence, the goal is to optimize the growth for long and straight tubes.

To avoid bundles we payed much attention on small and well dispersed catalyst particles. The catalyst is composed of $FeNO_3$, $MoCl_2O_2$ and AlO_2 nanoparticles of 4 nm size (obtained from Sigma-Aldrich). It is suspended in 2-propanol. When new catalyst is prepared it is sonicated overnight. Then it is always sonicated in a high-power bath-sonicater for half an hour before use. This is to ensure good dispersion and to avoid bundles during CVD growth. The samples (Si wafers with 400 nm SiO_2) are sonicated in acetone (10 min) and IPA (5 min) as well as placed in a UV-ozone cleaner for 10 min. Spinning at $4'000$ rpm for 40 s, two droplets of catalyst are added when maximum speed is reached.

Other gases are tested as ethylene or acetylene. An example is shown in Figure C.6. These gases decompose at lower temperature and thus the problem of amorphous carbon can be reduced. Temperatures between 750 and 900° C were tested. As catalyst $FeNO_3$ or evaporated Fe layers were used. But all our experiments with such processes ended in multi–walled nanotubes or in bundles.

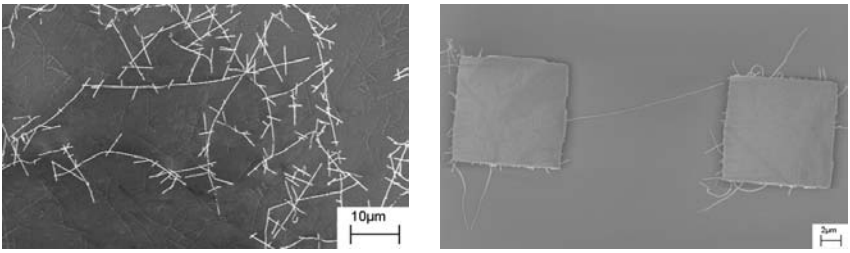
From band structure calculations (Appendix A.2.4) it is expected that one third of all nanotubes are semiconducting. For several CVD runs with the



(a) (b)

(c) (d)

Figure C.5: SEM pictures of CNTs grown by CVD at 900° C (a), 950° C (b), 1000° C (c) and 1050° C (d). Feeding gas was methane, the catalyst was $FeNO_3$, $MoCl_2O_2$ and AlO_2.



(a) (b)

Figure C.6: SEM pictures of CNTs grown by CVD with etylene. Parameters: T=900° C, catalyst: Fe layer equivalent to 5 Å thickness, patterned to islands in case of (b). Flow: 600 sccm Ar, 400 sccm H_2, 2 sccm C_2H_4. Growth time: 5 min.

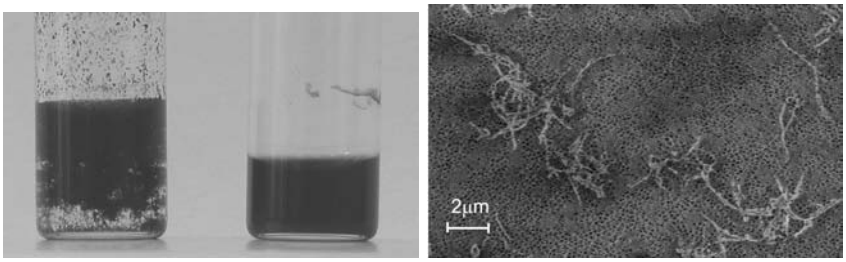
Table C.1: Table on CVD runs

CVD run	metallic	semiconducting	unclear
4.7.06	21	19	27
24.4.06	0	7	5
4.4.06	6	1	2
24.2.06	16	2	4
2.11.05	1	3	14
28.9.05	6	9	2

standard methane process many tubes were contacted and characterized. Tubes were called metallic if the current varies less 5 % within a gate voltage range of $-10 - 10$ V, they are called semiconducting if the current varies by more than two orders of magnitude. Otherwise they are called "unclear". The statistics is shown in Table C.1. The two runs with much more metallic tubes than semiconducting ones seem to be dominated by multi–walled nanotubes or bundles. These two runs were performed with methane gas from a different supplier and with an old quarz tube. These might be the reason for the unusual outcome.

C.3 Alternative fabrication approaches

Different approaches were tested to fabricate FETs devices by deposing nanotubes from liquid. Nanotubes tend to bundle very much. Surfactants are needed to separate them. It has been shown that ss-DNA can act as surfactant [168]. We tested DNA as surfactant as it could be modified to directly implement specific sensing experiments. Using a ss-DNA sequence of 30 T's, CNTs were solved in an aqueous NaCl solution. When CNTs are floating in a NaCl solution and ss-DNA is added, they suspend immediately. Stored in the fridge it stays for months. A photograph of solved CNTs is shown in Figure C.7(a).



(a) (b)

Figure C.7: (a) HipCo CNTs dispersed in H_2O with 0.1 M NaCl without (left) and with ss-DNA 30-T (right). (b) SEM image of DNA solved CNTs on an aluminum filter.

By simple adsorption the tubes with DNA can be dispersed on a silicon wafer with top oxide using the following recipe:

1. 100 μg SWCNTs in 400 μl NaCl (0.1 M).
   Tested material: High Pressure Carbondioxide (HiPCo) grown SWCNTs from Professor Richard E. Smalley at Rice University
2. sonicate for 90 min at high power, shake with mixing-tool before and after sonication, and eventually in between

3. add 100 μg ss-DNA (30 - T) solved in 100 μl NaCl (0.1 M)
4. sonicate 90 min at low power, ice - cooled
5. centrifuge for 60 min at 13000 rpm
6. incubate for 5 - 10 min on SiO_2 wafer, which was treated before in UVO for 30 min or functionalized with APTES (amino-propyl-triethoxysilane) as described in Appednix C.6
7. rinse slightly with some droplets of water.

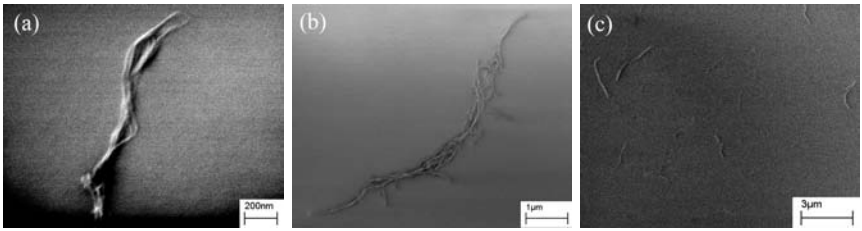
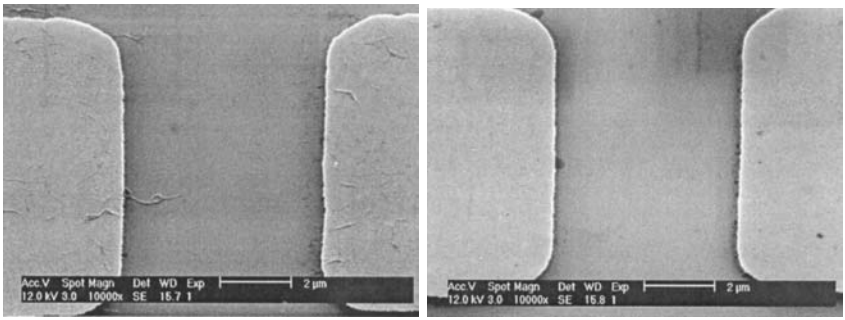


Figure C.8: HipCo CNTs with ss-DNA as surfactant deposited as described by the recipe in this Section. The sonication time in recipe point 4 (after adding ss-DNA) was chosen to be 30 min (a), 60 min (b) and 90 min (c). Whereas there are big bundles at lower sonication time, small bundles or even individual tubes dominate for 90 min sonication.

Shaking and sonicating the solution before adding the DNA helps to cut CNT clumps into small pieces which is important so that the DNA can access the tubes nicely. When DNA is added, one should sonicate at low power. Time and power have to bee adjusted to reach high yield of individual tubes. If the time is chosen too short, tubes ar not yet dispersed as shown in Figure C.8. For longer sonication times the tubes start to bundle again as DNA is efficiently cut into small pieces. UV ozone cleaning of the wafer before deposing the CNTs ensures that the solution wets the wafer all over. Rinsing after incubation helps to wash the salt away, but one should avoid washing the NTs away. To be able to incubate

the small amount of about 20 μl for 5 - 10 min we put it in a chamber with high humidity.

Nanotubes could be bound specifically on gold pads. ss-DNA (30 T) was assembled via a thiol end group on gold pads. Then the pads were incubated with a solution of DNA solved SWNTs for 1 h. As one can see in Figure C.9(a) the nanotubes stick specifically to gold. But most of them were still bundled. On bare Au pads they do not stick.



(a) (b)

Figure C.9: Au pads with (a) and without (b) ss-DNA functionalization. CNTs stick only on the pad with DNA.

The tubes we got (High Pressure Carbon dioxide (HiPCo) grown SWCNTs from Professor Richard E. Smalley at Rice University) were too short to be contacted. But the approach of assembling nanotubes could be followed in principle. Self assembled CNT FETs have been reported recently [169, 170].

Carbon nanotubes solved by ss-DNA were used to make nanotube networks. A strongly diluted solution was sucked trough an Al filter with nanopores by vacuum. By the amount of solution the density of the film could be adjusted. Low density of filtered CNTs are shown in Figure C.7(b). Excess DNA was washed away repeatedly by pure water. The films were transferred to a PET substrate by a PDMS stamp. All these

procedures are in analogy to the process of SDS solved carbon nanotube films by [171]. The network was contacted by silver paint or silver epoxy. The contact region was protected by wax for working in liquid and applying a gate voltage by electrolyte–gate (see Section 5.5.2). But working in liquid is not possible as the tubes start to float as soon as they are in contact with water. Note that CNT networks from SDS solved CNTs could be gated by an electrolyte as SDS solved CNTs are much less soluble.

C.4 E-beam lithography

For e-beam lithography a $200-600\,\mathrm{nm}$ thick film of polymethyl methacrylate (PMMA) was used as resist. The exposure was done either by a LEO Supra 35 at an acceleration voltage of $20\,\mathrm{kV}$ or by a JEOL JSM-IC848 at an acceleration voltage of $35\,\mathrm{kV}$. Moderate overdevelopment ensures good lift off of the resist and that the nanotubes are free of any resist as it seems that PMMA sticks much better on the tubes than on SiO_2.

C.5 Metal deposition

The deposition of SiO_2 and the metals was done by evaporation. The metal was heated and evaporated by an e-gun in a chamber at pressure of about $1\times10^{-7}\,\mathrm{mbar}$. One can chose the evaporation rate by adjusting the current passing the e-gun filament. The rate is measured by an oscillating crystal. To be sure that the heat of the melting metal does not affect the sample and to slow down diffusion processes it was cooled down to about $0°$ C, at least for evaporating contacts. When growing silicon oxide by this technique we do not have a well defined SiO_2, but SiO_x with unknown average number of oxide x. When evaporating Al a high evaporation rate of $\sim 5-10\,\mathrm{Å/s}$ was chosen to minimize oxidation during the evaporation process. For more noble metals lower rates of the range of ~ 1,Å/s were chosen. After deposing the metal, the resist was lifted off to free the sample from the metal wherever it had been protected. The lift off was

done by washing it in warm acetone immediately after the deposition and flushing it with a syringe.

C.6 Surface manipulation

To make SiO_2 hydrophobic it was covered with alkene-triethoxysilanes. Hydrophillic surface can be reached with amino-propyl-triethoxysilane. The deposition protocol is the following:

- alkene-triethoxysilane or amino-propyl-triethoxysilane in toluene solved by 1:10
- put sample and bottle with silane in chamber
- slowly open valve to vacuum pump, let it pump for 10 min
- close valve to vacuum pump, wait another 10 min
- vent slowly
- anneal at 80° C for 1 h so that the layer can rearrange to form a nice monolayer.

APPENDIX D

List of Symbols

Symbol	Description	Unit
C_d	General depletion capacitance	F
$C_{d,nw}$	Depletion capacitance of nanowire	F
C_g	Total capacitance between gate and nanowire or nanotube including depletion capacitance	F
$C_g^\star$	Total gate capacitance per unit length	F/m
C_g'	Total gate capacitance per unit area	F/m^2
C_{NT}'	Quantum capacitance of CNT	F/m
C_{ox}	Capacitance between gate and semiconductor	F
$C_{ox}^\star$	Oxide capacitance per unit length	F/m
C_{ox}'	Oxide capacitance per unit area	F/m^2
$C_{d,sub}$	Depletion capacitance of the substrate wafer	F
C_s	Semiconductor capacitance	F
e	Elementary charge $1.6 \cdot 10^{-19}$ C	C

(continued)

Symbol	Description	Unit
E_c	Bottom edge of conduction band	eV
E_f	Fermi energy	eV
E_g	Energy of band gap	eV
E_i	Intrinsic Fermi level	eV
E_v	Top edge of valence band	eV
G	Conductance 1/Resistance	$1/\Omega$
g_m	Transconductance of a FET: dG/dV_g	$1/\Omega$
h	Height of silicon device layer or nanowire	m
h_s	Height of charge carrier sheet	m
L	Length of silicon nanowire	m
n	Carrier density per volume in 3D material	m^{-3}
n	Carrier density per length in 1D material	m^{-1}
N_a	Density of acceptor dopants in silicon	$1/\mathrm{cm}^{-3}$
Q_{ox}	Charges within the gate oxide: Fixed charges near the interface to the Si and and oxide trap states and mobile ionic charges	C
S	Subthreshold swing	mV/dec
V_{fb}	Flat band voltage	V
V_g	Voltage applied to the gate of a transistor	V
V_{sd}	Voltage applied between source an drain contacts	V
V_{th}	Threshold gate voltage. In MOSFET and NW FET defined as onset of strong inversion, in CNTFET defined as gate voltage required to align the Fermi level with the conduction band edge $E_f = E_v$.	V
ΔV_g	Hysteresis between up and down ramp	V
W	Width of silicon nanowire	m
W_d	Depletion width	m
ε_0	Permittivity in vaccuum	F/m
ε_{H_2O}	Relative dielectric constant of water	
ε_{Si}	Relative dielectric constant of silicon	
ε_{SiO_2}	Relative dielectric constant of SiO_2	
ε_r	Unspecific relative dielectric constant	

(continued)

Symbol	Description	Unit
λ	Debye screening length	m
μ	Mobility	cm^2/V-s
μ_h	Mobility of holes	cm^2/V-s
μ_e	Mobility of electrons	cm^2/V-s
σ	Conductivity	$1/\Omega$
ϕ_m	Metal work function	V
ϕ_s	Semiconductor work function	V
Ψ_B	Fermi level with respect to intrinsic level in bluk, $\lvert E_f - E_i \rvert / e$	V
Ψ_s	Surface potential with respect to bulk	V

List of Figures

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Publication List

Paper

- M. Gräber, M. Weiss, D. Keller, S. Oberholzer, and C. Schönenberger, "Mapping electron delocalization by charge transport spectroscopy in an artificial molecule," *Annalen der Physik*, vol. 16, no. 10, p. 672, 2007.

Talks

- Dino Keller, Oren Knopfmacher, Michel Calame and Christian Schönenberger, "Molecular Sensors based on Silicon Nanowire Field Effect Transisotrs," Talk at Sensirion, The Sensor Company, Stäfa CH, July 25 2007.
- Dino Keller, Oren Knopfmacher, Michel Calame and Christian Schönenberger, "Molecular Sensors based on Silicon Nanowire Field Effect

Transisotrs," Talk at seminar on mesoscopic physics, Basel, July 2 2007.

- Dino Keller, Soufiane Ifadir, Jürg Furer, Michel Calame, and Christian Schönenberger, "Single Wall Carbon Nanotubes for Sensing Purposes," Talk at the E-MRS Spring Meeting 06, May 31 2006.
- Dino Keller, "Carbon Nanotubes: On Molecules that modulate their electronic conductance," Talk at the seminar for molecular electronics, Basel, February 24 2006
- Dino Keller, Soufiane Ifadir an Jürg Furer, Gunnar Gunnarsson, Michel Calame, and Christian Schönenberger, "Exploring Carbon Nanotubes for Sensing Purposes," Talk at Seminar at UCLA in the group of G. Grüner, August 30 2005.
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Poster contributions

- Dino Keller, Soufiane Ifadir an Jürg Furer, Michel Calame, and Christian Schönenberger,"Exploring Carbon Nanotubes for Sensing Purposes," Poster at the International Conference of Nanoscience and Technology (ICN+T) 2006, Basel, Switzerland, August 2 2006.
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